INTELLECTUAL POWER AWARE ROUTING(IPAR) METHODOLOGY FOR CONFIGURING NOC ARCHITECTURE

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Abstract:
Recently, System On Chip finds its applications in the hard-real time fields like Medical, Tele-Emergency, Automotives, Hospital management systems. These areas require more attention in terms of power and intelligence. To meet this above criterion, System on Chip Architecture itself needs the redefinition in terms of Core Interconnection architectures. Nowadays Implementation of Network On Chip(NoC) is popular for SoC but meeting the Power efficiency and intelligence in NOC routing is a strained challenge among the researchers. Hence we propose the new algorithm called Intellectual Power-Aware Routing(IPAR) for making the NoC flexible and scalable for the SoC architectures which can be further implemented for the Hard-Real Time Applications.

Keywords: IPAR, NoC, SoC, interconnection, Hard Real-Time Systems, Power Efficiency, Scalable.

I. Introduction

System on Chip (SoC) grown into a complex form due to which the number of cores has been incorporated for the heterogeneous embedded applications. But increase in the number of cores will make parameters such as speed, energy and performance also to be more and more complex. To meet this criterion, Network-On-Chip design has been proposed as the solutions for the communication between the 'n' numbers of the cores in the single CPU. In recent times, communication between the cores is established by the data network interface and the control network interface. Maintaining the performance and the communication among the CPU cores are significantly complex and routing algorithms has been proposed for effective communication. The most Recent algorithm is being adaptive shortest path determination among the cores[1] but the implementation for the power-efficient is still remaining on the darker side of the research.

The main objective of this work is to design a power-efficient and intellectual algorithm that can be suitable for the Network-On-Chip(NoC) architecture. The proposed algorithm works in the mechanism called IDM(Intellectual Distance measurement) in which the packets have been routed from the source cores to the destination core by selecting the least power and the distance between the cores. The Algorithms makes use of power consumption in accordance with the distance. The paper has been organized in the following manner, In Section II, related works have been reviewed. In Section III, the NoC framework has been focusedSection IV discusses about the proposed work with its Power model.

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II. Related Works:

Adaptive Fuzzy based Routing algorithms for the NoC in SoC has been discussed by Masoud Dehyadegari et.al [1] where it explains the adaptive fuzzy rules for deciding the power consumption in the cores. But the fuzzy rules sets have been formulated for a certain threshold and deals with read and write operations. Power Distribution in NoCs through a Fuzzy Selection has been discussed by Nastaran Salehi et.al[2]. The author explains the implementation of the Fuzzy controllers for effective power control mechanisms to reduce the average delays and decrease the power consumption.

The Implementation of the Intelligent mapping algorithms for NoC has been discussed by M.Taassori et.al[3]. This work describes the advantages of the Fuzzy based mapping techniques in the NoC and also the usage of Genetic algorithms and Simulating Annealing algorithms for the decent decrease in power consumption and the average delay in the NoC. A fuzzy-based power-aware routing algorithm for a network on a chip has been discussed by Salehi Arash Dana et.al[4] which clearly explains the selection of the best routing path by the removal of the congestion areas in the NoC. E.B. Nejad et.al [5] describes the fuzzy-based routing and Scheduling algorithms for the Input selection by the NoC based on the principle of priority logics. M.Li et al. presented a static XY algorithm with congestion condition to route the NoC[8]. The local information is used to identify the neighbouring routers to decide the next hop.

III. NoCFramework

The number of cores and IP modules are present in System on Chip, to interconnect all those things a bus-based interconnected architecture is required to improve the required performance. But this bus-based interconnection does not provide the required latency, bandwidth and also it consumes more power. To overcome these problems switching based interconnection is embedded to interconnect the IP modules, namely NoCs. On comparing with the bus-based interconnection, the NoC design has different routing strategies for efficient communication of IP modules. The network on chip architecture includes links, router and network interface. The link that physically connects the IP modules, which provides the communication between them. The router that implements the communication protocol, which receives the packets from shared links and that information is forwarded to another shared link or core. The communication protocol defined with certain policies to handle the common situations like packets arriving at the same time or disputing the same channel, avoiding deadlock and livelock situations, reducing the communication latency, increasing the throughput, etc. The network interface or network adaptor makes the logical connection between network and IP cores. A routing function determines the path of a packet from its source node to the destination node. Most networks use deterministic routing schemes for simplicity. In contrast, Intellectual Power-Aware Routing(IPAR) enhance the throughput and latency with low power.

IV. Proposed IPAR Working Methodology

The working mechanism of the IPAR algorithm can be split into the two-phases which follows Intellectual Distance Mechanisms(IDM) and Power AwareMechanisms(Write/Read operations).

A. IDM Phases: As the First Step, Since NoC is connected with the different masters and the slaves. The master sends the Control Signal to find the one-hop distance regarding the Slave's position. During this phases, different X and Y Coordinates of the slaves will be identified and it searches the best and least distance of the slave with respect to the master. The intellectual

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shortest distance between the cores and the master will take place at this phase. In this phase, placements of the different cores have been known to the master after mapping in the SoC. The Placements of the different cores are shown in Figure 1. The IDM phases include the selection of the cores to participate in the network by the distance between the master and Slaves. The distance can be measured by the X-Y Coordinates between the Cores and by forming the intellectual rules minimum distance will be calculated.

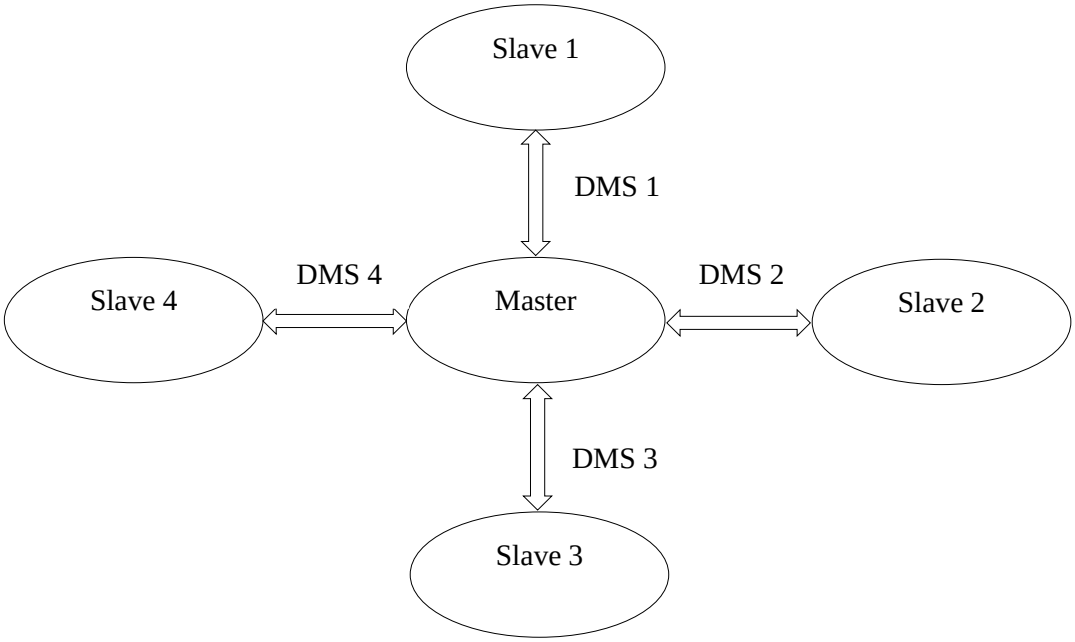

Fig.1 Mode of Connection between the Master and Slaves in NoC

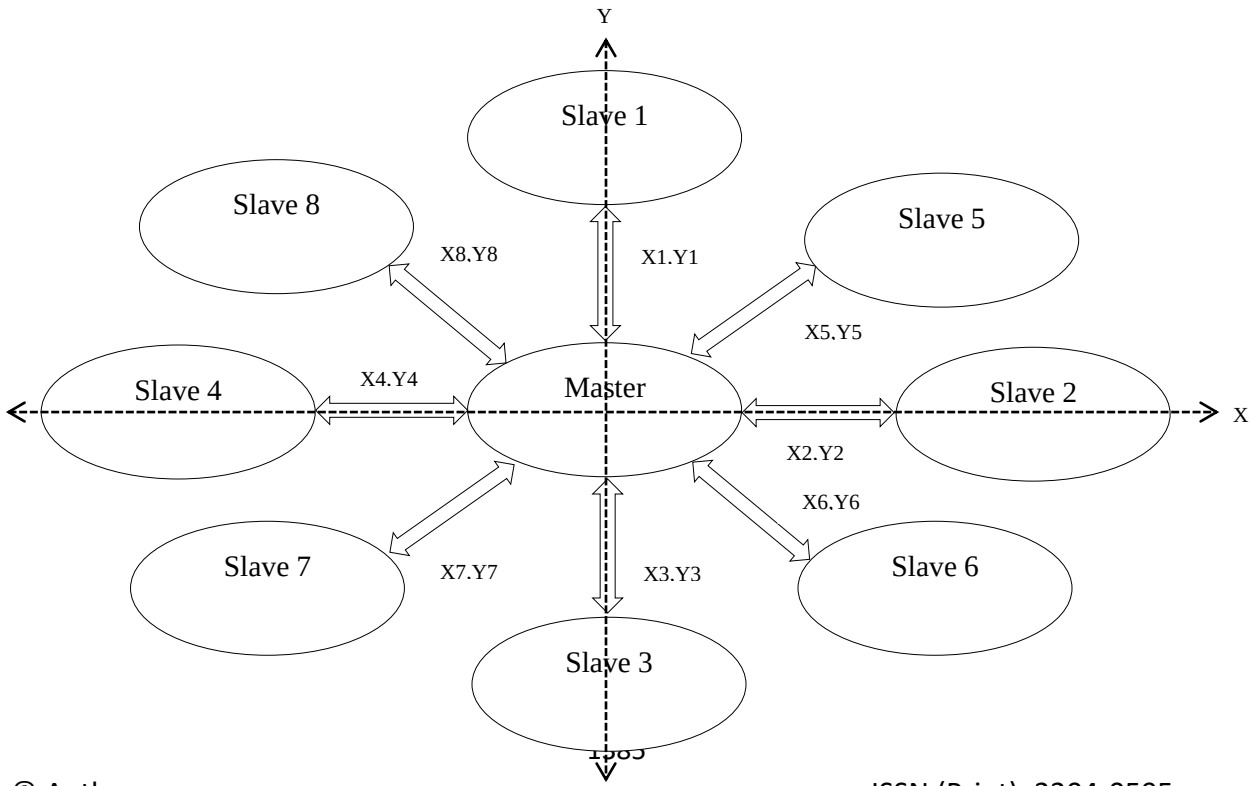

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Fig.2 Placements of the Different Cores in the SoC communication between the Master and the Slave

Figure 3 shows the slave core which is at X5,Y5 has been selected as the core since the sixth co-ordinate core are situated in the minimum X-Y distance. It shows the Selection of the Cores by the Master(IDM Phase) in which the green colour shows the On state, the Yellow colour shows the next shortest distance cores for the next phase and the other cores in the off state. Figure 4 Shows the Selection of the Next Cores by the Master(IDM Phases) in which the green colour shows the On state, Red colour shows the OFF state. .

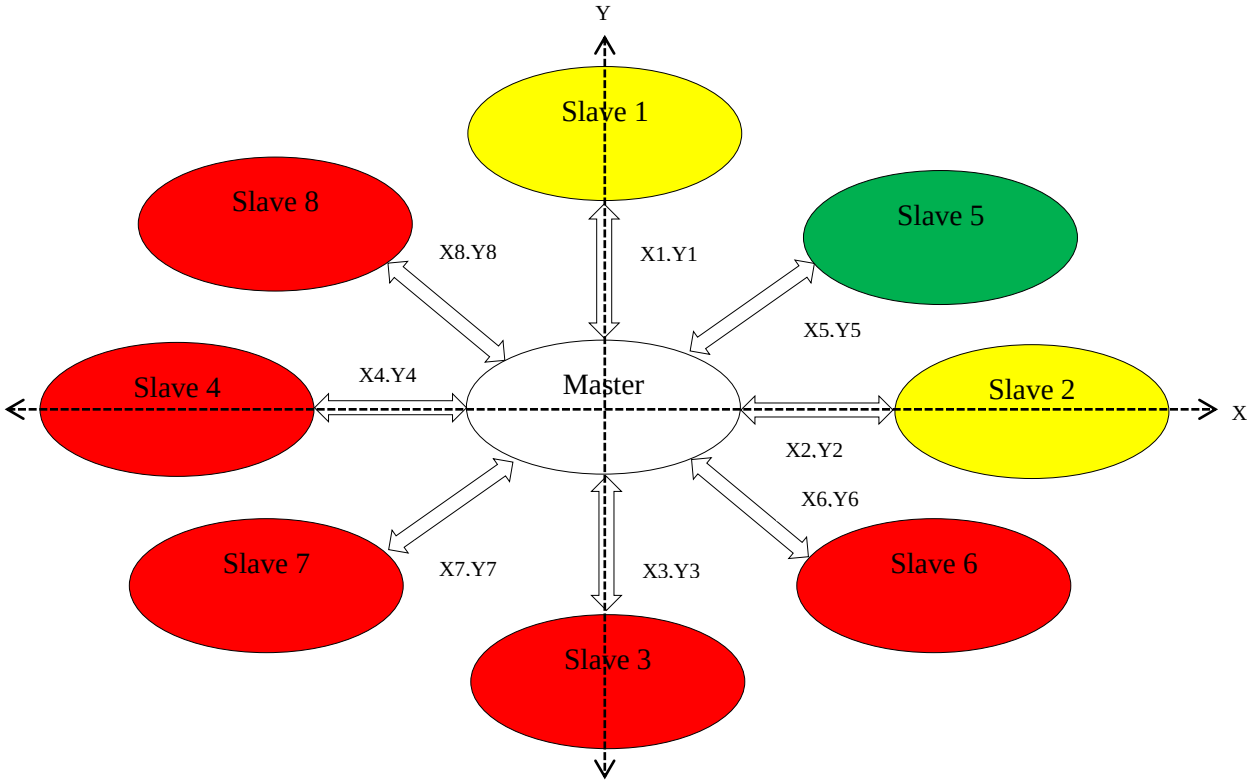

Fig.3Selection of the Cores by the Master(IDM Phase)

B. Power Aware Cycles of Operations: In the next phase, the least distance cores will be selected by the master for read and write operations. The read and write operations will take place between the master and the cores depends on the energy to be calculated depends on the least distance. This new model is known to be Power-Aware read/Write Operations. This Phase communication between the Master and the LDM–Slaves will be taken care and all other remaining cores will not participate in the networking. Figure 5 Energy consumption for the cores depends on the distance in which the Power-aware read and write cycles will take place between the cores and the Master.

V. Power Models

The power models for the network on chip interconnection can be modelled as follows :

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$$Pt=Pwr+Prd+PL+Px \quad \ldots\ldots\ldots (1)$$

Which can be modified as

$$P(k) =\{(J(i) \times \sum S.A(k) \}/T \quad \ldots\ldots (2)$$

Where, S.A(k) - Switching activity operations
N(k) - Number of Operations
Prd - Power for read operations
Pwr - Power for write operations
PL - Power for Links
Px - Power for the Bus Implementation
J(i) - Functional with respective to I terms

Now the mathematical model for the IDM can be given as follows as

$$D(M,S) = Min(X,Y) \quad \ldots\ldots\ldots (3)$$

Where, D(M,S) - Distance between the master and slave
Min(X,Y) - Mininmum X-Y Co-ordinates between the Master and Slave.

Again the Distance model can be rewritten as follows as

$$D(M,S) = Dt = Min(X,Y) \quad \ldots\ldots\ldots (4)$$

Where, Dt =least Distance between the Master and Slave
By combining all above equations, Intellectual rules can be formulated as follows as

$$P(M,S) = \begin{cases} Pm & when\ Dt = D \\ 0 & when\ Dt \neq D \end{cases}$$

$\ldots\ldots\ldots$ (5)

Where P(M,S) - Power required for the master and Slave Operations.

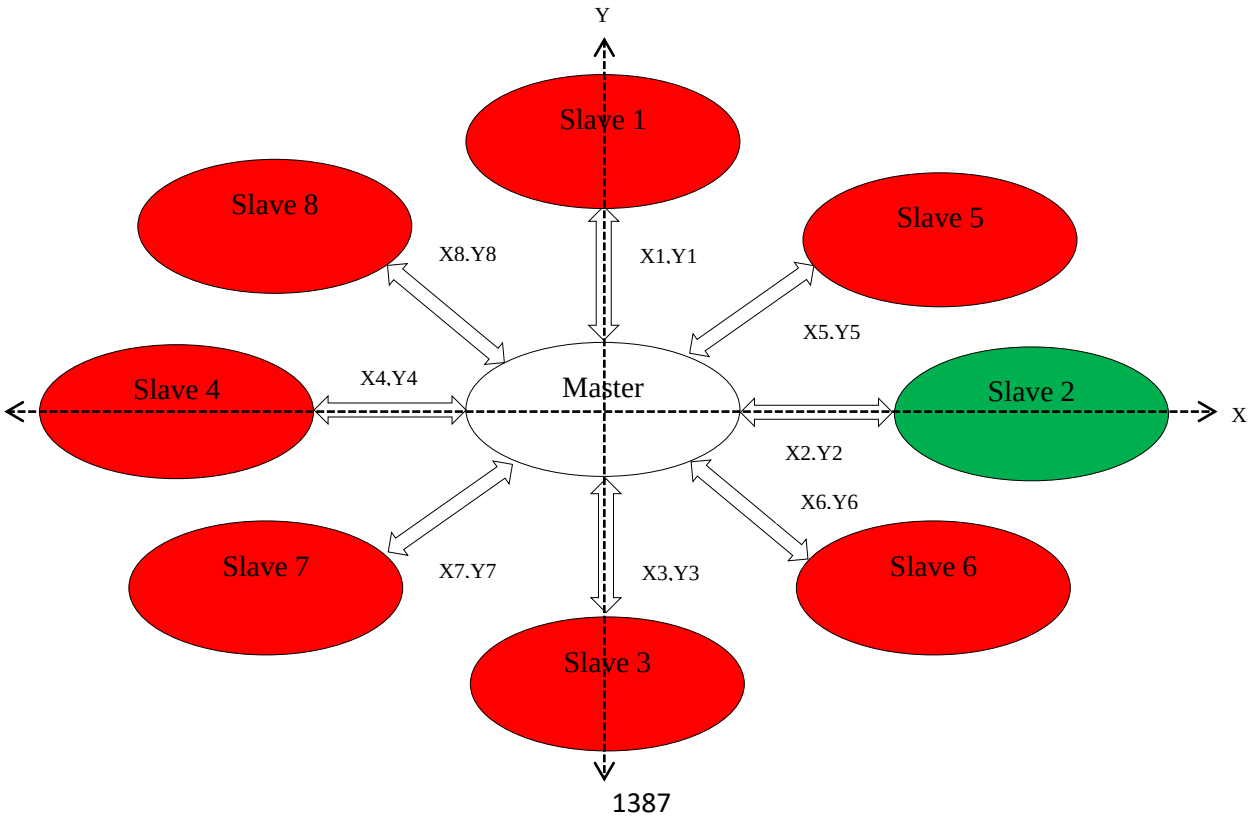

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Fig.4Selection of the Next Cores by the Master(IDMPhases)

Again the Power Aware Read and write Cycles can be calculated by following equations:

$$Ptd = \sum D(M,S) \times Pm \times PL \times Px \quad \ldots\ldots\ (6)$$

Where, Ptd - Total Power consumed in the cores between the master and the slaves.
For the PAW Operations Power can be calculated as follows

$$Pw = Ptdx\ Nw \quad \ldots\ldots\ (7)$$

$$Pr = Ptdx\ Nr \quad \ldots\ldots\ (8)$$

Where, Pw is the Power for Write Operations and Pr is the Power for read Operations and Nw/Nr are the No of Cycles for Read/Write Operations.

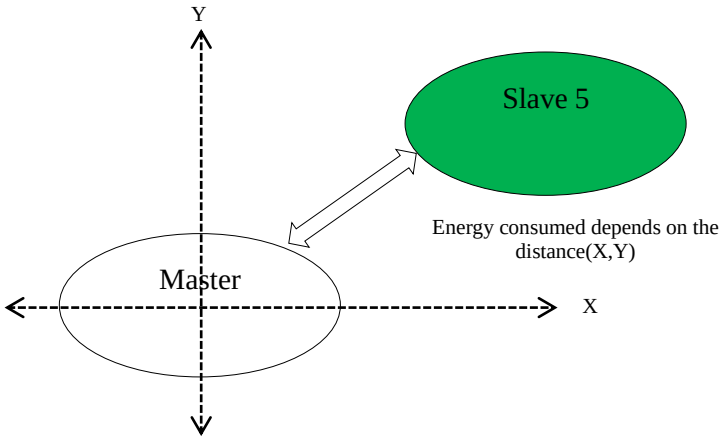

Fig.5 Energy consumption for the cores depends on the distance

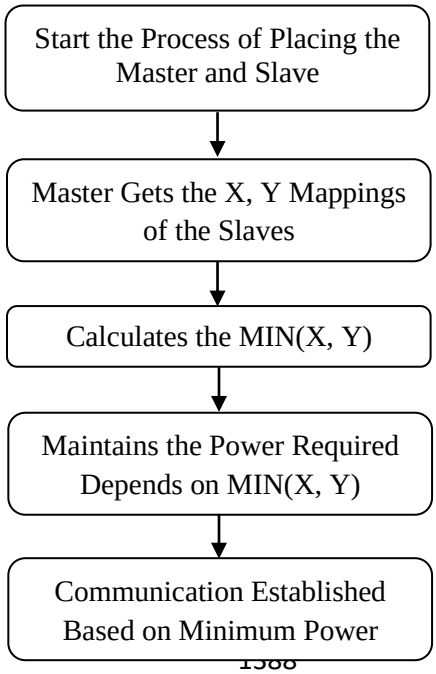

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Fig.6 Flowchart for Description ofIDM mechanisms in NOC Communication

The algorithm can be defined as follows for the mechanisms can be defined taking the one master with the number of the slaves. The basic working mechanism is shown in figure 6. Initially, the master and slave nodes are placed based on the given task. Master gets the X, Y mappings of all the slaves and the distance between each slave is calculated. The minimum distance is identified and the communication between master and slave will be established based on the minimum power and minimum distance slave.

VI. Results and Discussion

The methodology was implemented on the Xilinx Zynq SoC platform with Verilog programming. The Zynq SOC has Dual ARM-Cortex Boards and the One FPGA Cores in which the ARM Core has been taken as the Applications master and IPs has been tested using FPGA Synthesis. Power calculated for the single-core communication between the master and slave is given as follows. The Comparative Analysis shows the Power Analysis of the different IP Communication using IDM concerning the Adaptive Intelligent algorithms such as Fuzzy logic is shown in Table 1. The average power consumption of the testbed has been calculated by running the testbed continuously by getting the Inputs from the sensors connected. The algorithm has been tested with the SoC for the different IPs communication and the throughput/efficiency has been calculated based on the equation given as follows as

TP = Time taken for the execution of single IPapplicationXPower taken for the IPCommunication

$$Performance = \frac{TP}{Total\ time\ taken}$$

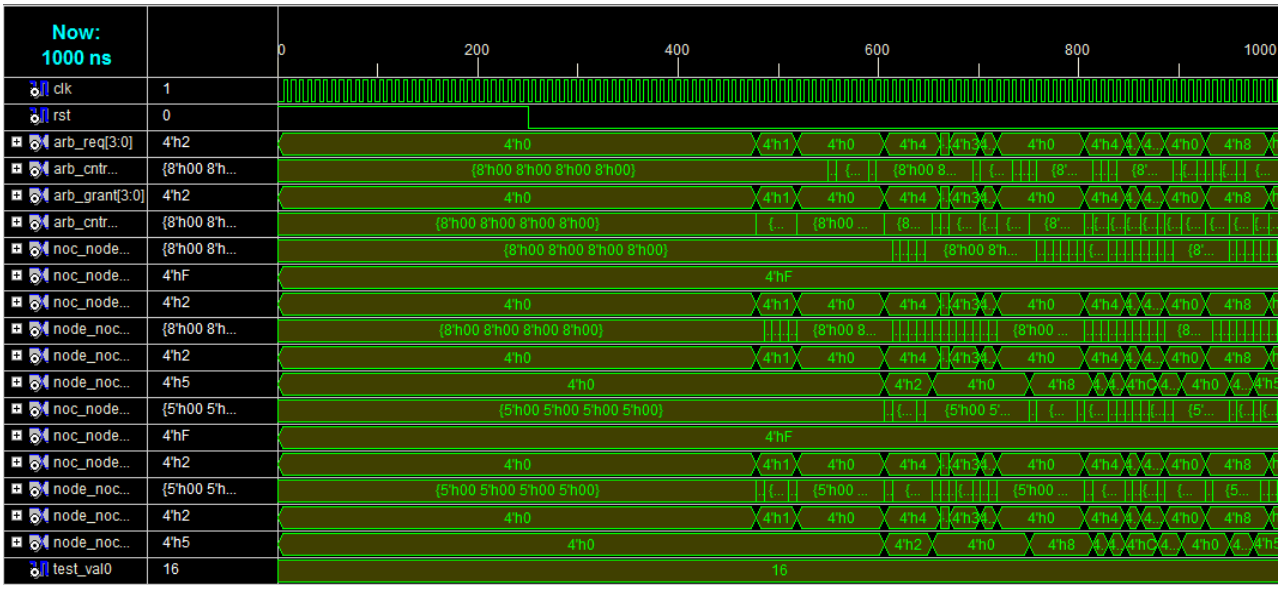

Fig.7 Simulation Results shows the PAW and PAR Cycles of Operations

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Table 1 Power consumption of the Single Core communication between the Master and Slave

Parameters	Adaptive Fuzzy	Proposed IPARSystem
Total Power	1.031nW	0.367nW

The performance of the system is calculated by running the device for several hours. The performance results suggested that our proposed method consumes less power when compared with an adaptive fuzzy algorithm.

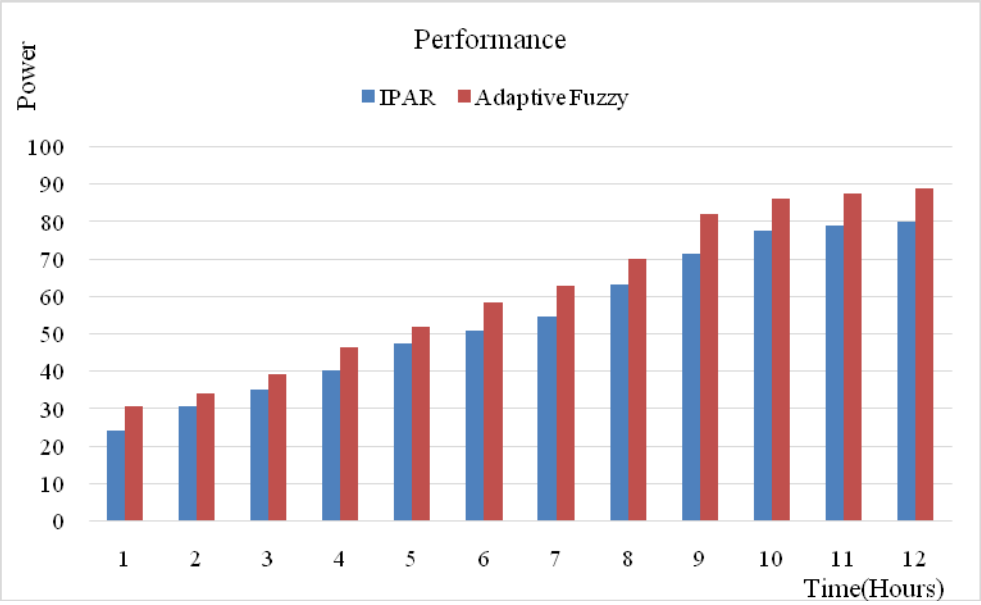

Fig.8 Performance comparison (Time vs Power)

VII. Conclusion

The Algorithm has been designed for heterogeneous emergency real-time rescue applications where the Intelligence of the power is mandatory. The power consumption for this NOC when integrated with SoC can be used for the different emergency cases such as in healthcare, defence and telecommunication systems. The algorithms prove to be vital and it shows the pivotal increase in the 20-25% decrease in the power when compared to the other algorithms.

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