# 9T SRAM CELL WITH MT-SVL TECHNIQUE FOR LEAKAGE POWER REDUCTION

Kothamasu Jyothi [1], Aswini Valluri [2], P. Vijaya Lakshmi [3], Sarada Musala [4]

Dept. of Electronics and Communication Engineering

Vignan's Foundations for Science Technology and Research, Deemed to be University, A.P, India.

kothamasujyothi1993@gmail.com[1], aswini.valluri@gmail.com[2], posanivijaya@gmail.com[3], sarada.marasu@gmail.com[4]

**Abstract: With the technology scaling there is a decrease in transistor size and increase in number of the transistors per a chip. It causes tremendous increase in complexity and the power dissipation of circuits. This paper mainly focuses on reduction of leakage power dissipation in SRAM 9T cells by employing multi threshold self controllable voltage level circuits (LSVL & USVL). The Simulation results show that with the employment of MT-SVL technique, leakage power is being reduced compared to the improved SVL technique. The overall simulation is done with CMOS 180nm technology, using the tool of Cadence Virtuoso.**

Keywords—SRAM, leakage power,MT-SVL, Improved SVL, 180-nm technology.

## I. INTRODUCTION

With the advancement in the CMOS technologies, usage of the portable devices is increasingas they are small in size, easy to carry and reliable.In integrated circuits 40% of the power from the supply is consumed due to standby power dissipation[1].These days it is possible for the designer to design the chip with, low power consumption, high speed, less area and high packing density[2]. The technology node estimated to be scaled down to 7-32 nm scale in near future with advancement of FINFET. As we are emerging to nanometer scale devices, certain features of device are deteriorated: power dissipation increases as number of transistors per chip increases, gain decreases, sensitivity to small fluctuation during manufacturing process and short channel effects. These parameters affect the reliability and yield of chip[3].

Such portable handheld devices need memory like SRAM, as they are faster and there is no need to refresh the memory periodically [4].This is particularly true for microprocessors in which the sizes of on-chip cache are developing with each generation in order to increase the speed of the processors and main memory [5]. Hence the requirement for SRAM is increasing with its great use in System-On-Chip as well as high performance VLSI circuits.In the designing of these memory cells leakage power dissipation is the major concern and data stability is degraded. The power dissipation is mainly of two types: switching and standby power dissipation. Mainly it is necessary to reduce the leakage power which reduces overall power dissipation drastically in SRAM.

Typical SRAM consists of four transistors organized in such a mannerthat two inverters are attached back to back for storing bit information, followed by two pass transistors in order to control the storage bit during the write and read operations. Apart from the storage it has two stable states which denotes 0 and 1 [6].

Leakage power dissipation in CMOS circuits is based on two reasons: Firstly leakage power is directly proportional to the number of transistor in CMOS circuit and secondly due to temperature dependence of the CMOS circuit. To reduce the leakage power a novel technique multi-threshold self controllable voltage level (MT-SVL) is introduced.

The paper is organized as follows: Section II provides working of 9T SRAM cell. Section III is about details of existing work with improved upper and lower SVL technique. Section IV is about the proposed method MT-SVL technique for a SRAM 9T cell to reduce standby power. Section V reflects the simulation results obtained using cadence virtuoso tool and lastly section VI is conclusion to the work done.

## II. 9T SRAM CELL

The advantage of SRAM 9T cell is thatit simultaneously reduces leakage power along with enhancementin the data stability. 9T SRAM cell completely separates the data withthe bit lines as shown in Fig.1.The read process is performed by using a separate read signal line(RD). During read process, RD is made high and the write signal line(WL) is made low which deactivates the two access transistors (M5 & M6).The operation of M7 and M8 transistors is carried by depending on the information stored inthe storage nodes. BL and BLB are discharged and charged based on the storage nodes data. During the write process, WL is made high and RD is made low making M9 to be in cutoff mode. This is how read operation and write operation are carried out in SRAM 9T cell.
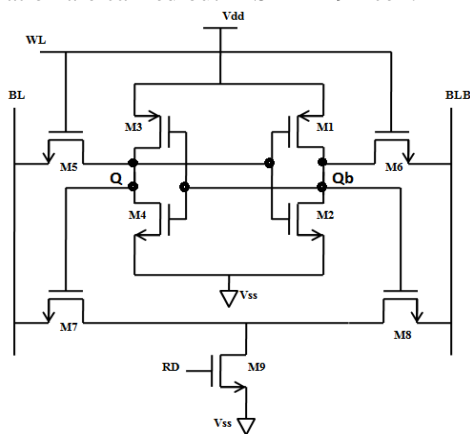


Fig.1 SRAM 9T cell

### III.  SELF-CONTROLLABLE VOLTAGE LEVEL 9T SRAM CELL

In SVL method,the load circuit is operated with a full supply voltage in an active mode and a fraction of supply voltage when load circuit is in standby mode to reduce the standby power dissipation[7]. Therefore, in standby mode, an alternate path is made toslightly lower the voltage and relatively higher the voltage to the load by using an ON switch.Hence,$V_{ds}$ of the OFF state MOSFETs reduces the substrate voltage $V_{sub}$ which further increases the $V_{th}$due to decrease in thesub threshold current.Self-controllable voltage level (SVL)circuits are classified into 3 types. They are (a) Lower SVL circuit, (b) Upper SVL circuit and (c) UL-SVL [8]. To reduce the leakage power to more extent an Improved SVL technique is designed.

Improved Upper and lower self-controllable voltage level circuit (I-USVL, I-LSVL) is shown in the Fig. 2[9]. In standby modePM1 is OFFto make sure that it providesa high resistance path between Vdd&Vd as shown in Fig.2(a). NM1 is ON and

produces a voltage of Vdd-Vth. NM2 transistor acts like a resistor soas to reduce the current through upper SVL circuit. Thus it reduces the leakage current. The operation is similar for Improved Lower selfcontrollable voltage level circuit (I-LSVL) as shown in Fig.2(b). LSVL circuit provides power to the load circuit in an active mode using NMOS. Also LSVL ensures to supply Vss to the load in standby mode using PMOS transistors [10].
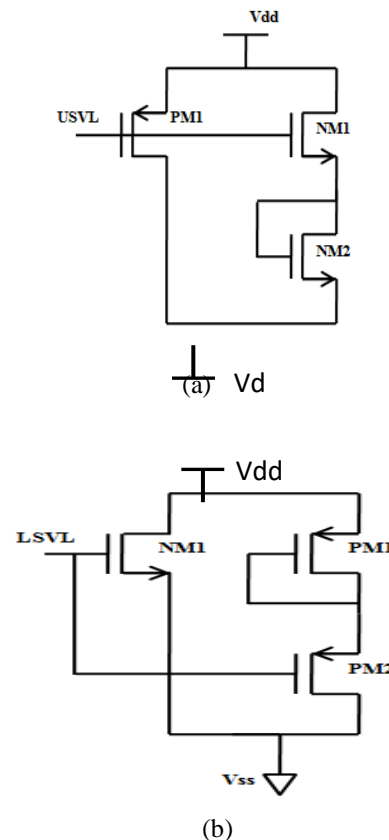


(a)



(b)

Fig.2:  (a) I-USVL &(b) I-LSVL circuit

### IV.  PROPOSED MULTI THRESHOLD SVL 9T SRAM CELL

Multi threshold upperself-controllable voltage level circuit (MT-USVL) design is as shown in Fig.3(a).PM1 transistor provides full supply voltage to load circuit in active mode.NM1 supplies -Vth to the load circuit in standby mode and NM2 acts as a resistor. In active mode, PMOS is on and both NMOS high threshold voltage transistors (Vth) are off providing full supply voltage to the load circuit. In standby mode PMOS is off and both NMOS transistors are on and diode transistor (NM2) acts as resistorwhich in turn reduces current. NMOS transistors are high Vth transistorwhich does not turn for small voltages.Hence supply voltage is reduced for load

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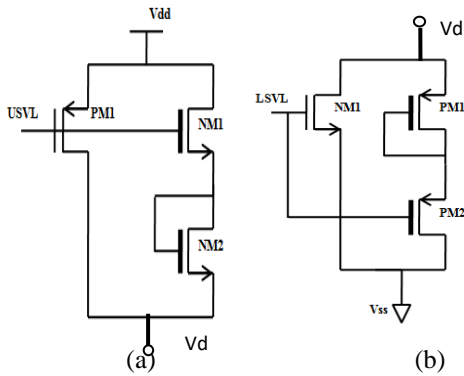circuit in standby mode thereby reducing the leakage power.



Fig.3: (a) MT-USVL &(b) MT-LSVL circuits

Multi threshold lower self-controllable voltage level circuit (MT-LSVL) is designed as shown in Fig.3(b). In active mode, NMOS is ON and both PMOS transistors with high threshold voltage (Vth) are OFFproviding power to the load circuit. In standby mode NMOS is off and both PMOS transistors are on and diode transistor (PM1) acts as resistor in turn reducing thesub threshold current. NM1 provides high impedance path between Vd and Vss.The MT-LSVL provides Vss to the load in standbymode.AsPMOS transistors are high Vth transistors they turn on for very small voltages.

The proposed method MT-SVL technique is being applied to 9T SRAM cell to evaluate the power dissipation in active and normal mode. The MT-SVL circuit links the SRAM cell to either Vss or Vdd during the active mode of operation. In a standby mode, MT-SVL circuit links the SRAM cell to either reduced supply voltage or increased ground potential.Thus with the aid of high Vth transistors the standby power dissipation is reduced.

Fig.4, Fig.5 and Fig.6 gives the implementation of MT-USVL, MT-LSVL and MT-ULSVL techniques respectively for a 9T SRAM cell. The simulation results thus obtained for the 9T SRAM cell using the Multi T technique is presented in Section V.

Table1: MT-SVL operation

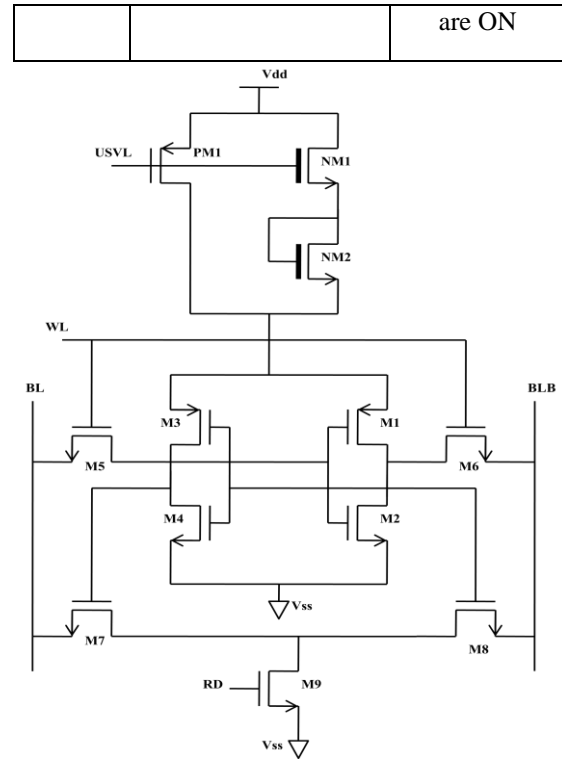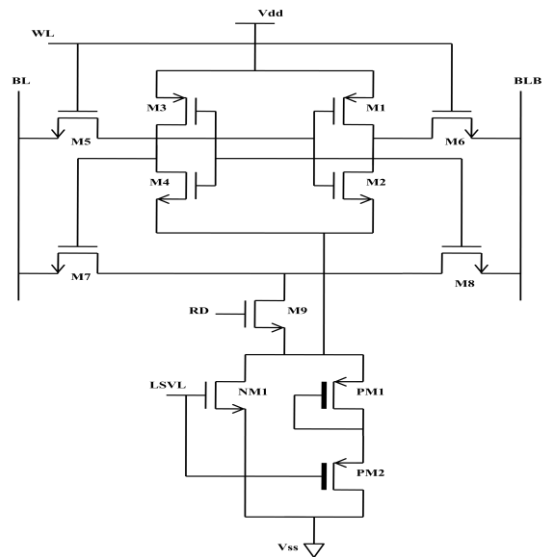| MODE | MT-USVL | MT-LSVL |
|---|---|---|
| Active mode | PM1 is ON NM1,NM2 are OFF | NM1 is ON PM1,PM2 are OFF |
| Standby mode | PM1 is OFF NM1,NM2 are ON | NM1 is OFF PM1,PM2 |



Fig.4:  9T SRAM cell with MT-USVL



Fig.5: 9T SRAM cell with MT-LSVL

## V.    SIMULATION RESULTS

The transient analysis of the proposed MT-USVL, MT-LSVL and MT-ULSVL circuits is shown in Fig.7, Fig.8 and Fig.9 respectively. This section represents the comparison results of the proposed method of MT-LSVL, MT-USVL and MT-ULSVL with 9T SRAM cell as shown in Fig.10, Fig.11 and Fig.12 respectively. Table.2 gives the comparison of the ULSVL method at various supply voltages.
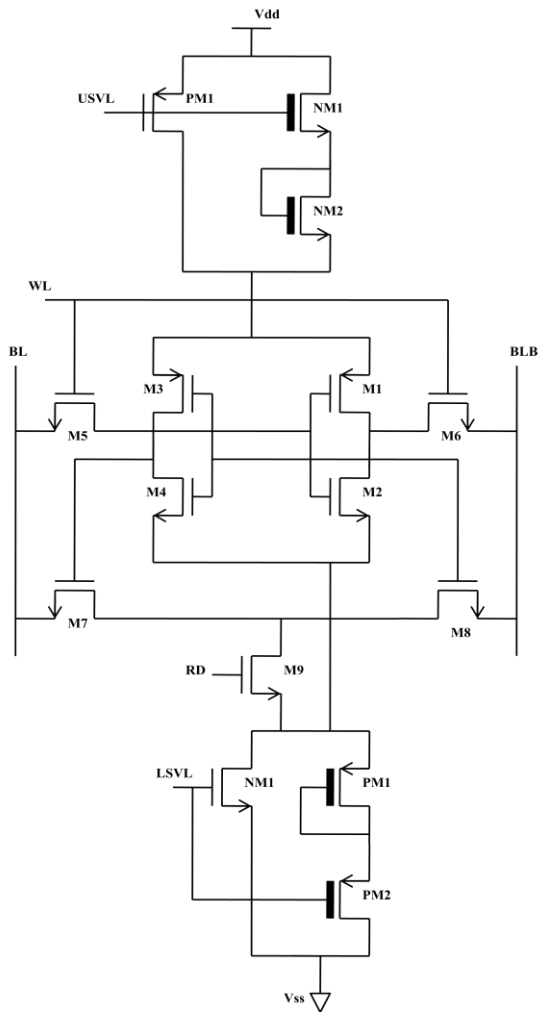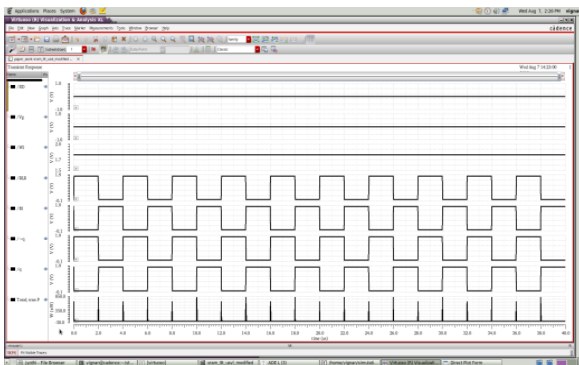
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Fig.6:  9T SRAM cell with MT-ULSVL



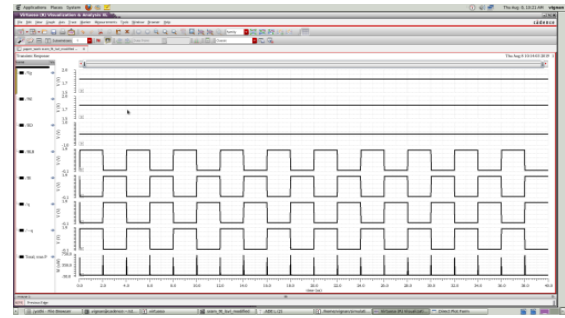Fig.7: Transient response of the proposed MT-USVL



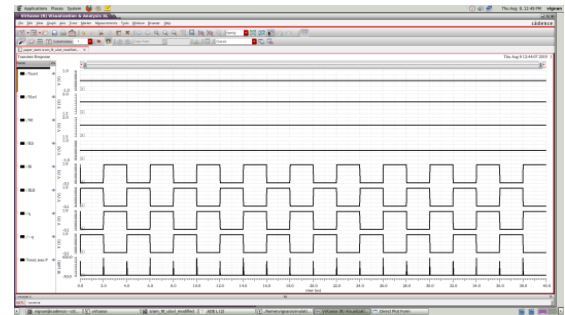Fig.8: Transient response of the proposed MT-LSVL.
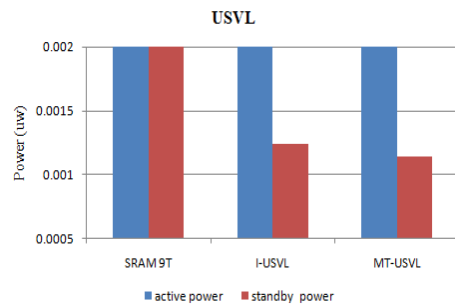


Fig.9: Transient response of the proposed MT-ULSVL.



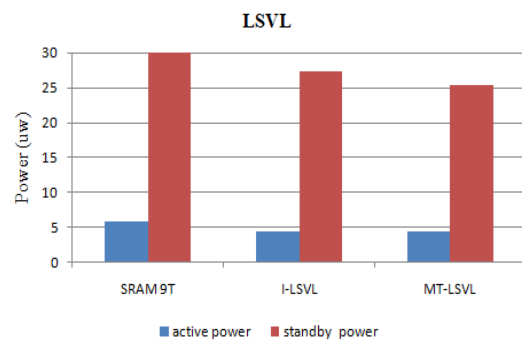Fig.10: Active and Standby power comparison of USVL circuit at 1.8V



Fig.11: Active and Standby power comparison of LSVL circuit at 1.8V
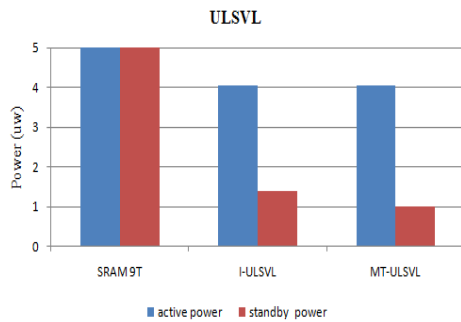
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Fig.12: Active and Standby power comparison of ULSVL circuit at 1.8V

Table2: Delay, Active and Standby power of MT-ULSVL at different voltages

| Supply Voltage(V) | Delay (ns) | Active Power(uw) | Standby Power |
|---|---|---|---|
| 1.8 | 2.2075 | 4.058 | 1.014uW |
| 1.7 | 2.5295 | 3.479 | 903.4pW |
| 1.6 | 2.983 | 2.946 | 790.7pW |
| 1.5 | 3.5455 | 2.45 | 23.61nW |
| 1.4 | 4.2005 | 1.985 | 646.6pW |
| 1.3 | 4.954 | 1.574 | 599.9pW |

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## VI.     CONCLUSION

ISVL and MTSVL techniques play crucial role in reducing leakage power in low power SRAM cells. In this paper the performance of SRAM 9T is analyzed and simulated with ISVL and proposed MTSVL techniques using 180nm technology files. The advantage of high Vth transistor in standby mode is that it reduces the power dissipation when the load circuit is off. Simulation results show that there is a decrease of 27% standby power with the proposed method. This MT-SVL technique can be applied for the low power SRAM designs including 6T, 7T, 8T, 10T cells.

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