Three-Phase Three-Level Isolated DC-DC Soft Switching Converter For Solar Applications

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Abstract: Three-level isolated DC-DC converter is an attractive topology in high input voltage applications, which can provide the voltage stress of the power devices to only a half of the dc voltage and also reduce the size of dc filter requirement. But major limitations in the existing three level ZVS converter topologies are brought out with an increased inductance in the primary side and it required to provide complete ZVS of all primary devices down to light loads. By employing an external inductance in the primary of the transformer, total leakage inductance of the transformer increases which is required for realization of soft switching of the converter switches but there are some disadvantages of connecting external inductance in the primary of the transformer. To overcome all these drawbacks, the three-phase three-level isolated DC-DC soft switching converter has been proposed in order to reduce voltage and current stresses. This converter topology requires less number of control switches and operates with an asymmetrical duty cycle control. The proposed three level DC-DC converters provide two- level voltage waveform before dc output filter, which significantly reduce the size of dc output filter. The proposed work has been implemented using MATLAB/SIMULINK and the performance of the proposed converter is verified through simulation results.

***Keywords*: Three-phase, Three-level, isolated DC-DC Converter, Switching losses. Zero voltage Switching (ZVS), duty cycle control.**

1. Introduction

To overcome the limitations of single phase three level DC-DC converters, three-phase three-level isolated DC-DC soft switching converters are considered in order to reduce voltage and current stresses. In DC-DC power conversion, three-phase full bridge PWM dc-to-dc soft-switched converters have placed considerable importance. A three phase three-level topology has been proposed in [1], [14] for inverter application to minimize the voltage stress to half of the dc input voltage. The three level converter has been used for realizing a dc-to-dc converter in [2], [3]. In [4], the phase-shifted PWM is used to provide soft commutation and it is a simple control structure and compact system having high power density and at high power levels, the components of the converter provides considerable current stress.

Three-level converter is an attractive topology in high input voltage applications, which can provide the voltage stress of the power devices to only a half of the dc voltage [5]. To further minimizes the voltage rating of devices for three-phase three-level and three-phase full-bridge PWM DC-DC converters were proposed in [6], [7], as a combine configuration of half-bridge three level converter and full-bridge three-phase converter. The symmetrical duty cycle control was used in the converter [6], and the converter has the advantages including lower voltage stress on devices, voltage source characteristic and soft-switching capabilities for output stage. A phase-shifted PWM control strategy was employed in the converter [7], as a result, the devices can provide ZVS and ZCS without any additional auxiliary components. The common advantages of three phase three level DC-DC converters specified above are the employment of a three-phase transformer and inverter configuration, even though the voltage stress on devices can be minimized, the power devices result in the larger overall cost and increased complexity of control circuit.

The other alternative were developed in [4], [8], these topologies uses a three-phase high frequency transformer coupled to a three-phase inverter and to a three-phase high frequency rectifier. The advantage of this topology increase the output and input current frequency by a factor of three as compared to full-bridge converter and smaller rms current in the power components and reduction of cores. Even though, it indicates satisfactory features, soft commutation has not been provided, which limits the power density and the switching frequency. The use of asymmetrical duty cycle in three-phase DC-DC converter was developed in [9], [10] to provide ZVS commutation of all devices for a wide load range. Analogously to the full-bridge converter, the selected topology undergoes conduction losses in the secondary stage, because two series diodes carry the load current. Hence, involvement of a three-phase high efficiency rectifier and a three-phase DC-DC converter seems to be an optimal placement to applications that demand low output voltages and high current levels. It provides an increment in the output current and input current

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frequencies by a factor of three as that of full bridge converter. This will results in lower current ratings for the components and a reduction of size of isolation transformer. But, switching devices experience the control structure and high voltage stress is also involved. In order to overcome these drawbacks, a converter topology consists of a three-phase three level Phase shift PWM converter consists of six devices operates under ZVS and six devices operates under ZCS has been presented in [11]. But, the control duty cycle range of the converter is from 0 to 120°. In order to obtain the rated voltage, the converter must be overrated by 33%. To overcome this drawback, a new three-level dc-to dc Phase shift PWM converter is considered in [3], [12] consists of secondary rectifier is a centre-tapped full-wave current tripler. This makes to considerable reduction in the size of the dc output filter as compared to conventional full bridge topology. For the same power at a specified voltage level, the current carried by each switch is minimizes to one-third as that of converter in [13]. Therefore, a lower rated switch will be used for a high-power application and it leads to good thermal management as total power dissipation gets distributed over more number of switches. Hence, the rms value of input current is less as compared to single-phase version for the same power level and dc-link voltage [13]. The soft switching of devices based on ZVS is provided by energy stored in the transformer leakage inductance [14] and soft switching of devices based on ZCS is provided by placing tapped filter inductors at the output side of transformer [15]. The mechanism of dc output filter having a tapped inductor provides reduction in circulating current during a freewheeling interval, which results with reduced conduction losses.

To satisfy the needs for high conversion performance, some solutions take resonant three-phase converters where soft switching can be provided, including the resonant LCC-type converter proposed in [16] and resonant LCL-type converter in [17]. The improved resonant converter provides ZVS condition under wider load range and higher converter efficiency. The wide changes in switching frequency should be used in the applications with high input/output voltage range. The other alternative schemes are the three-phase non resonant soft-switching converters. The three-phase DC-DC converter with asymmetrical PWM was presented in [18], [19], in order to provide ZVS commutation for all devices and control the output voltage, the lower and upper commutation cell devices are focused to different current stresses. All the topologies mentioned are usually suitable for medium voltage level, for the devices still sustain the whole input voltage and will provide high voltage stress in high input voltage applications.

In this research work, the three-phase three-level isolated DC-DC soft switching converter has been proposed in order to reduce voltage and current stresses. This converter topology requires less number of control switches and operates with an asymmetrical duty cycle control. The proposed three level DC-DC converters provide three- level voltage waveform in the primary side of transformer, which significantly reduce the size of dc output filter.

2. Three-Phase Three-Level Isolated Dc-Dc Converter:

The circuit diagram of three phase three level converter is shown in Figure 1. The delta/star connected three-phase transformer is used with low turns ratio and low VA rating. The inductances L_{ra}, L_{rb} and L_{rc} are used along with transformer leakage inductances L_{lka}, L_{lkb} and L_{lkc} to make wider ZVS range. The freewheeling diodes D_{f1} and D_{f2} are used along with flying capacitor C_{SS}. The diodes D_{R1}-D_{R6} are the rectifying diodes. The dc output filter consisting of L_f, C_f and R_0 is the load resistance.

2.1: Proposed three-phase three-level (TPTL) ZVS isolated DC-DC converter:

The switching pattern of the original control algorithm and modified control algorithm are as shown in Figures 2 and 3. From Figure 2, it is clear that the duty cycle of all the control switches are equal and conduction period of each control switch is 120°. The specified duty cycle of each control switch is in the range of 0.167 to 0.33. The duty cycle of control switch is varying with the dc input voltage and load, the incoming control switch cannot be exactly turned on at the instant of collector to emitter voltage zero within the operational period. Hence, the switches are operating under hard switching and produce considerable switching losses. In order to provide ZVS commutation in the switches, the interleaved control switches are to be designed in a complementary manner with proper dead time and it is similar to the control mechanism used in the asymmetrical half bridge converter. Therefore the control switches S_1, S_3 and S_5 are receiving complementary pulses of control switches S_4, S_6 and S_2. The control pulses for the asymmetrical scheme are as shown in Figure 3.

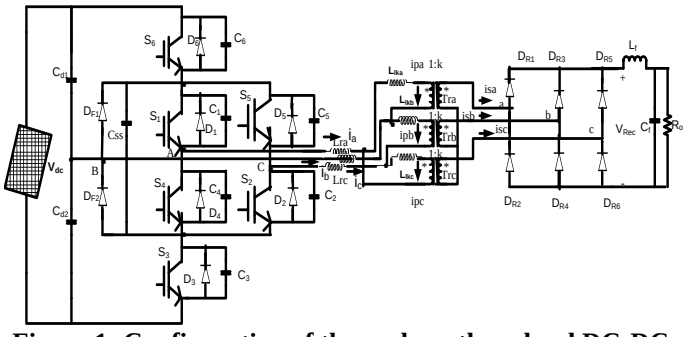

Figure 1: Configuration of three phase three level DC-DC converter

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Table 1: Comparison of Proposed converter with existing converter

Type of Element	Three-phase Three-Level DC-DC converter topology [6]	Proposed Three-phase Three-Level DC-DC Converter Topology
Control switches	n* 4	n * 2
Diodes	n* 6	n* 4
Gate-Amp	n* 4	n * 2
Dc-Link Capacitors	n*3	n
Switching Losses	High	Low
	Where "**n** "is the number of transformer primary voltage levels, n=3	

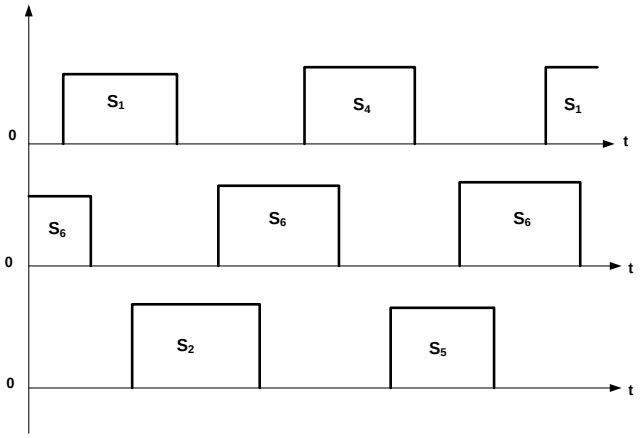

Figure 2: Symmetrical duty cycle control

Figure 3: Asymmetrical duty cycle control of proposed converter

Table 1 shows the comparison of proposed three-phase three- level DC-DC converter with conventional three-phase three-level DC-DC converter. From table 1, it is noticed that, the no. of control switches used in the proposed converter are less than the conventional converter.

2.2 Modes of operation:

The following assumptions are considered in TPTL DC-DC converter:

(i) The control switches and diodes are ideal

(ii) All inductances and capacitances are ideal

(iii) The output filter inductor should be large enough to make output current continuous and constant throughout the switching period.

(iv) The primary side inductances in each phase of the transformer is identical. ie., $L_{lka}=L_{lkb}=L_{lkc}=L_{lk}$, $L_{ra}=L_{rb}=L_{rc}=L_r$

(v) The intrinsic capacitors are equal. $C_1=C_2=C_3=C_4=C_5=C_6=C_r$.

The operational waveform of the proposed converter is shown in Figure 4 for asymmetrical duty cycle control. This converter has 18 operational modes and 7 operational modes are shown in Figures 5 to 11 and the remaining modes are symmetrical to first 7 modes in the switching cycle.

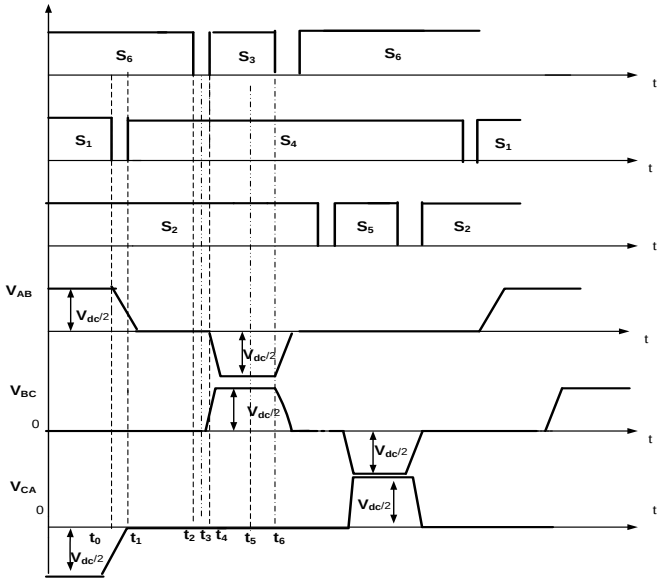

Figure 4: Operational waveforms of the proposed converter

The currents and voltages of transformer are listed as under:

$$V_{AB} + V_{BC} + V_{CA} = 0 \quad (1)$$

$$i_{sa} + i_{sb} + i_{sc} = 0 \quad (2)$$

$$\frac{di_a}{dt} = \frac{(d\, i_{sa})}{N_T dt} = \frac{v_{Llka}}{L_{lk}} \quad (3)$$

$$\frac{di_b}{dt} = \frac{(d\, i_{sb})}{N_T dt} = \frac{v_{Llkb}}{L_{lk}} \quad (4)$$

$$\frac{dc}{dt} = \frac{(d\, i_{sc})}{N_T dt} = \frac{v_{Llkc}}{L_{lk}} \quad (5)$$

Where N_T denotes turns ratio from primary to secondary of transformer. The voltage drop across transformer leakage inductance is deduced from (4.25) - (4.28) and is given by,

$$v_{Llka} + v_{Llkb} + v_{Llkc} = 0 \quad (6)$$

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Operational mode 1: (prior to t_0)

Before time $t=t_0$, the switches S_1, S_2, S_6 are on along with diode D_{f2} in the primary side and diodes D_{R1} and D_{R6} are operating in the secondary side as shown in Figure 5. The voltages $V_{AB}=V_{dc}/2$, $V_{BC}=0$ and $V_{CA}=-V_{dc}/2$. Based on equations (4.24), (4.25) and (4.29), the following voltages are obtained:

$$v_{pa} = \frac{V_{dc}}{2}, v_{pb} = 0, v_{pc} = -\frac{V_{dc}}{2} \quad (7)$$

$$v_{rec} = v_{sa} - v_{sc} = \frac{1}{N_T}.V_{dc} \quad (8)$$

Where V_{pi} denotes transformer primary voltage and V_{si} denotes transformer secondary voltage, the script 'i' denotes a, b, and c subscripts.

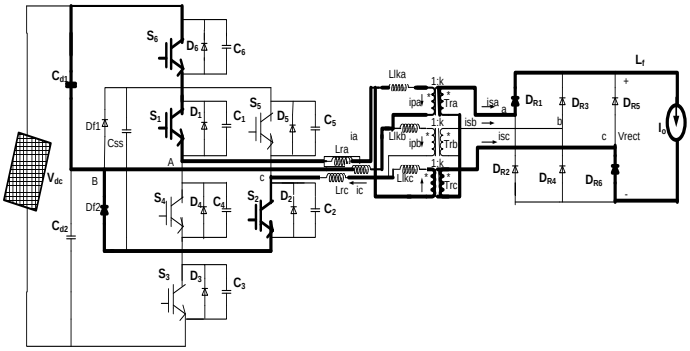

Figure 5: Equivalent circuit for mode '1' operation

Operational Mode 2: $t_0 \leq t < t_1$

At time $t=t_0$, the control switch S_1 is off. Thereby capacitor C_1 starts charging whereas the capacitor C_4 discharges linearly and hence the rectifying voltage will get reduced, as shown in Figure 6. The rising rate of voltage across S_1 is limited by the capacitor C_1. The voltage across C_1 and C_4 are as follows:

$$v_{C1}(t) = \frac{1}{C_{rN_T}} I_o(t - t_o) \quad (9)$$

$$v_{C4}(t) = \frac{V_{dc}}{2} - \left(\frac{1}{C_r N_T}.I_o(t - t_o)\right) \quad (10)$$

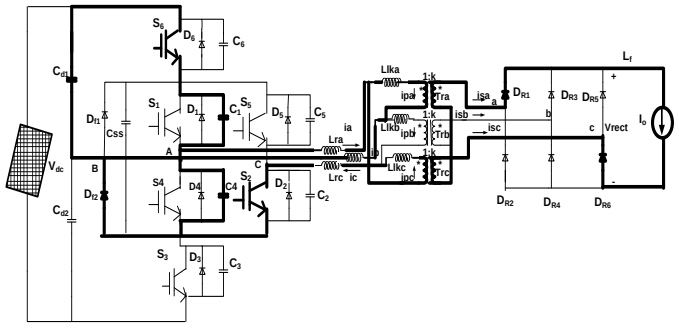

Figure 6: Equivalent circuit for mode '2' operation

At time $t=t_1$, the voltage across C_1 increases to $V_{dc}/2$ and the voltage across C_4 falls to zero. Hence the diode D_4 naturally conducts and rectifying voltage becomes reduced to zero.

Operation Mode 3: $t_1 \leq t < t_2$

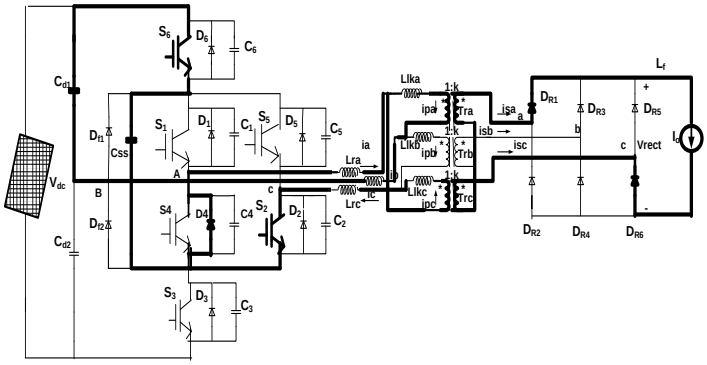

Figure 7: Equivalent circuit for mode '3' operation

The current flowing through C_1 is transferred to C_{SS} when the capacitor C_1 is totally charged and C_{SS} begins to charge. The voltage capacitor C_{SS} increases and it blocks the diode D_{f2} into off state, during this period, $V_{AB}=V_{BC}=V_{CA}=0$. The diode D_4 starts conducting and it makes zero voltage condition for turn-on of switch S_4. The diodes D_{R1} and D_{R6} are operating and rectifying voltage becomes zero, as shown in Figure 7.

Operation Mode 4: $t_2 \leq t < t_3$

At time $t=t_2$, the control switch S_6 is turn-off under ZVS and voltage V_{AB} rises in reverse polarity. If voltage V_{pa} is maintained constant then voltage polarity of L_{lka} is independent on current flowing through it. Thereby, the current i_{pa} will decrease and in this instant the load current cannot be provided. In this case, the diode D_{R3} starts conducting and current becomes commutates between diodes D_{R1} and D_{R3} as shown in Figure 8.

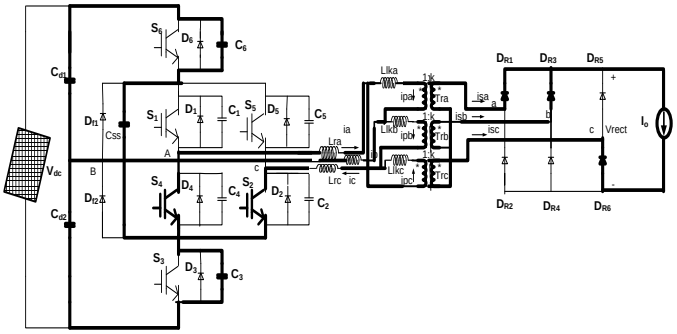

Figure 8: Equivalent circuit for mode '4' operation

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The voltage across C_3 and C_6 are as follows.

$$v_{C3}(t) = \frac{V_{dc}}{2} - (\frac{1}{2N_T}.I_0.Z_r.\sin[w_r(t-t_2)]) \quad (11)$$

$$v_{C6}(t) = \frac{1}{2N_T} I_0\, Z_r.\sin[w_r(t-t_2)] \quad (12)$$

$$i_A(t) = \frac{3}{2N_T}.I_0 + \frac{1}{2}\frac{1}{N_T}.I_0\cos[w_r(t-t_2)] \quad (13)$$

$$i_B(t) = -\frac{1}{N_T}.I_0\cos[w_r(t-t_2)] \quad (14)$$

$$i_C(t) = -\frac{3}{2N_T}.I_0 + \frac{1}{2}\frac{1}{N_T}.I_0.\cos[w_r(t-t_2)] \quad (15)$$

In this mode, the rectifying voltage becomes zero. Thereby, the voltage across capacitor C_3 decrease to zero and simultaneously D_3 starts conducting.

Operational Mode 5: $t_3 \le t < t_4$

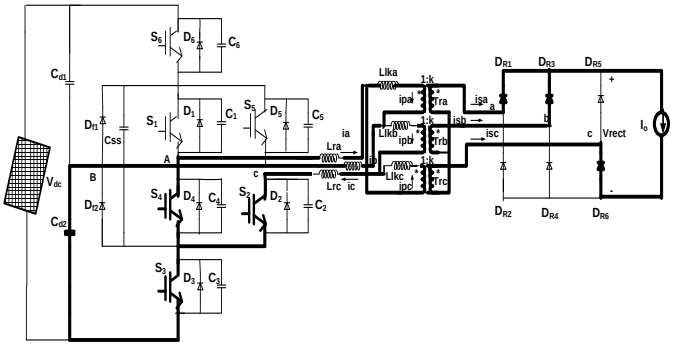

Figure 9: Equivalent circuit for mode '5' operation

The control switch S_3 is ready to turn-on under ZVS at any time after $t=t_2$ since the body diode D_3 is already on. In this mode, the switches S_2, S_3 and S_4 are conducting, thereby $V_{AB}=-V_{dc}/2$, $V_{BC}=V_{dc}/2$, $V_{CA}=0$. The rectifying diodes D_{R6}, D_{R1}, D_{R3} are conducting and rectifying voltage becomes zero as shown in Figure 9. The phase currents in the proposed converter during this mode are,

$$i_{pa}(t) = i_{pa}(t_3) - \frac{V_{dc}}{2L_p}.(t-t_3) \quad (16)$$

$$i_{pb}(t) = i_{pb}(t_3) + \frac{V_{dc}}{2L_p}.(t-t_3) \quad (17)$$

$$i_{pc}(t) = -\frac{1}{N_T}.I_0 \quad (18)$$

The line currents can be determined from (4.33) to (4.35) is as follows.

$$i_A(t) = i_A(t_3) - \frac{V_{dc}}{2L_p}.(t-t_3) \quad (19)$$

$$i_B(t) = i_B(t_3) + \frac{V_{dc}}{L_p}.(t-t_3) \quad (20)$$

$$i_C(t) = i_C(t_3) - \frac{V_{dc}}{2L_p}.(t-t_3) \quad (21)$$

From equation (4.39), the current i_{sa} flowing through D_{R1} will be falls to zero then diode D_{R2} conducts and diode D_{R1} turned off simultaneously. As compared to the primary voltage, the rectifying voltage is lost at time $t=t_{3,4}$. The loss of duty cycle is given by,

$$D_{loss1} = \frac{t_{3,4}}{\frac{T_{Sw}}{3}} = \frac{6.I_o.L_p}{N_T.V_{dc}.T_S} \quad (22)$$

Where T_s is the switching time period.

Operational Mode 6: $t_4 \le t < t_5$

During this interval, $V_{AB}=-V_{dc}/2$, $V_{BC}=V_{dc}/2$ and $V_{CA}=0$. The voltage and current expressions of the transformer during this mode are,

$$v_{pa} = -\frac{V_{dc}}{4}, v_{pb} = \frac{V_{dc}}{2}, v_{pc} = -\frac{V_{dc}}{4} \quad (23)$$

$$v_{rec} = v_{sb} - v_{sc} = \frac{3*V_{dc}}{2*N_T} \quad (24)$$

$$i_A(t) = \frac{1}{N_T}.I_o - \frac{V_{dc}}{2L_p}.(t-t_4) \quad (25)$$

$$i_B(t) = \frac{1}{N_T}.I_o + \frac{V_{dc}}{4L_p}.(t-t_4) \quad (26)$$

$$i_B(t) = -2.\frac{1}{N_T}.I_o + \frac{V_{dc}}{4L_p}.(t-t_4) \quad (27)$$

The current i_{sc} will flows through the diode D_{R6}. The diode D_{R6} is turned off, when the current i_{sc} falls to zero. At this time, the transformer primary and secondary currents are becomes zero as shown in Figure 10. The time duration of this state is given by,

$$t_{4,5} = \frac{4.L_P\, I_{o.}}{N_T.V_{dc}} \quad (28)$$

After this state, the switches S_2, S_3 and S_4 are conducting in the primary side and the diodes D_{R2} and D_{R3} conducting in the secondary side. The rectifying voltage becomes $k*V_{dc}$, and it is same as the rectifying voltage in mode 1. The equivalent circuit of this mode is shown in Figure 10.

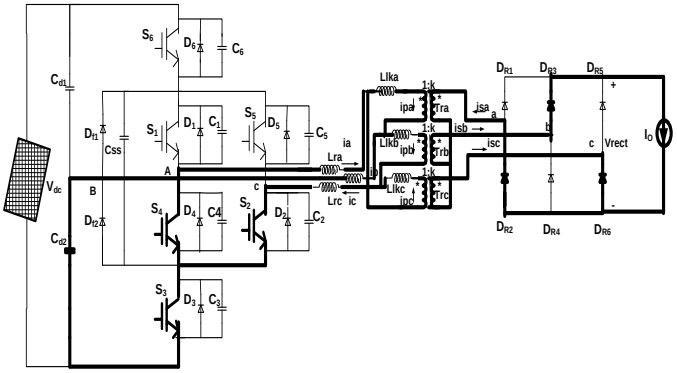

Figure 10: Equivalent circuit for mode '6' operation

Operational Mode 7: $t_5 \le t < t_6$

After mode 6, the switches S_2, S_3 and S_4 are operating in the primary side, the diodes D_{R2} and D_{R3} are operating in the

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secondary side and the rectified voltage becomes $\frac{1}{N_T}.V_{dc}$ which is same as mode 1. The equivalent of this mode is shown in Figure 11.

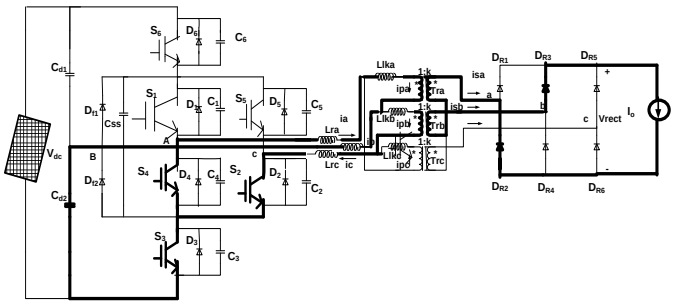

Figure 11: Equivalent circuit for mode '7' operation

2.3 Design equations:

The converter design indicates the design of values for C_{d1}, C_{d2}, C_1, C_2, C_3, C_4, C_5, C_6, C_{SS}, L_{lk}, L_f and C_f.

The output inductor should be large enough to make the output current should be continuous throughout the switching period and leakage inductance of transformer must be small enough to make the less reset time.

The capacitors C_{d1} and C_{d2} must be large enough to make the voltage division must be maintained as constant even when the change of input voltage and voltage spikes produced by the switching capacitances.

The resonant capacitor C_r (=C_1=C_2=C_3=C_4= C_5=C_6) must be selected in such a way that the minimum requirement for ZVS operation of control switch during turn-off. The large capacitance is required to hold the switch voltage closed to zero during current fall time of the switch (t_{fi}). The value of t_{fi} can be taken from the data sheet. The value of C_r can e calculated as,

Where I_p is the peak value of current flowing through the primary winding of transformers.

The capacitor C_{SS} can be determined based on parasitic capacitor C_r of switch

$$C_{SS} = \frac{C_r}{0.05} = 20 * C_r \quad (30)$$

The dc output filter elements are designed based on the following equations:

$$\Delta I_O = \frac{V_O * (1-k) * T_s}{L_f} \quad (31)$$

$$\frac{\Delta V_O}{V_O} = \frac{\pi^2 * (1-k) * f_r^2}{f_{sw}^2} \quad (32)$$

$$f_r = \frac{1}{2 * \pi * \sqrt{L_f * C_f}} \quad (33)$$

Where ΔV_O & ΔI_O are the acceptable ripple contents in the dc output voltage and current waveforms, V_O is the required dc output voltage, f_r is the resonant frequency, f_{sw}=($1/T_s$) is the switching frequency and k is the duty cycle of switch.

2.4 Realization of soft switching:

Before turning on the switches under ZVS, enough energy is required in intrinsic capacitors to fully charge or discharge them. At the time of transition of control switches S_2, S_4 and S_6 (shown in Figure in 4.45), the charging current in intrinsic capacitors is directly proportional to load current. Thereby, the switch voltages changes linearly and output filter inductance is used to provide required energy for ZVS condition of three switches.

In order to make zero voltage turn-on, the incoming switch intrinsic capacitor is fully discharged through line current during dead time. The ZVS condition of the switch is lost if the current used in equation (4.30) is below I_{omin} and it is given by,

$$I_{omin,\ S2,S4,S6} = \frac{V_{dc}\ C_r . N_T}{2t_d} \quad (34)$$

In order to achieve ZVS for the switches S_1, S_3 and S_5, the energy stored in the transformer leakage inductances and resonant inductances are used. The ZVS condition of switch is lost if the current below minimum current used in equations (4.31 and 4.32) is given by,

$$I_{omin,\ S1,S3,S5} = \frac{N_T . V_{dc.}}{Z_r} \quad (35)$$

3. Results and Discussion:

The parameters of the proposed converter circuit shown in Figure 1, are shown in table 2.

Table 2: Converter parameters

Name of the parameter	Value
Switching frequency, f_{sw}	10KHz
DC Input voltage, V_{dc}	100V
DC Output voltage, V_o	24V
DC Input capacitance, C_{d1}	200uF
Parasitic capacitor, C_r	10uF
Leakage Inductance of transformer, L_{lk}	25.4uH
Turns ratio of transformer (N_P:N_S), N_T	1:1
DC filter inductance, L_f	8.7mH
DC filter capacitance, C_f	10uF
DC load current, I_o	80A
Power Rating, P	2000W

Figure 12 show the gate pulses of the proposed converter switches. If the switches S_1& S_6 are used to make positive V_{AB} and switches S_3 & S_4 are used to make negative V_{AB}. If the switches S_2& S_3 are used to make positive V_{BC} and switches S_6 & S_5 are used to make negative V_{BC}. If the

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switches S_4, S_5 & S_6 are used to make positive V_{CA} and switches S_1, S_2 & S_6 are used to make negative V_{CA}. The primary voltages V_{AB}, V_{BC} and V_{CA} of all three transformers are displaced by 120º. The three-level voltages in the primary side of each transformer are 0, $V_{dc}/2$ and $-V_{dc}/2$.

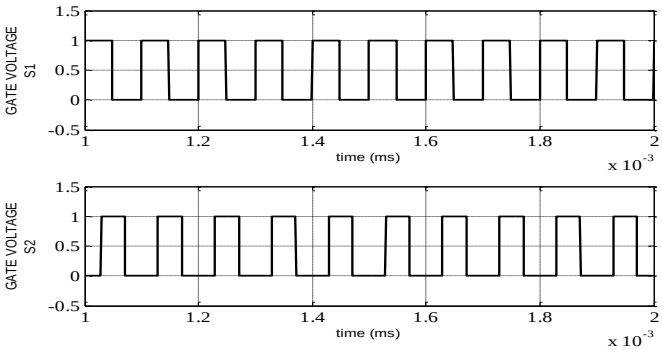

Figure 12 (a): Gate pulses for S_1 and S_2

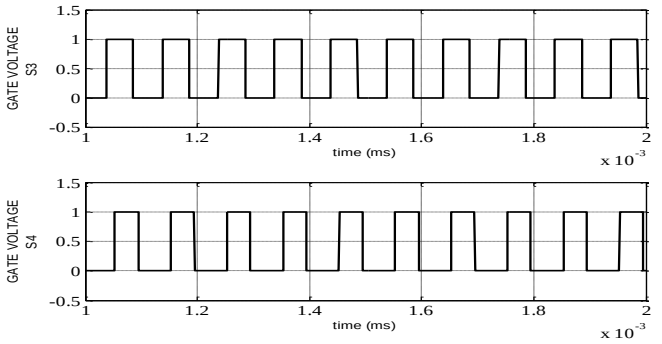

Figure 12 (b): Gate pulses for S_3 and S_4

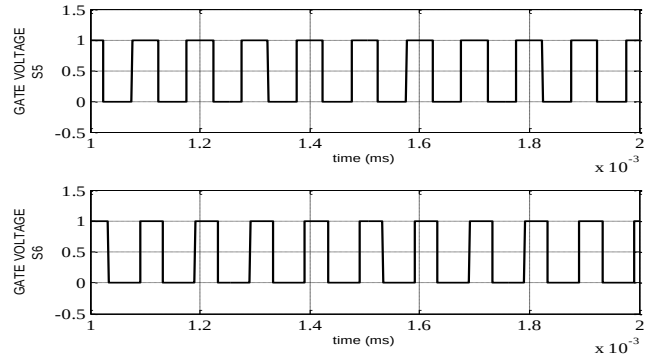

Figure 12 (c): Gate pulses for S_5 and S_6

Figure 4.48: Gate pulses for proposed three-phase three-level DC-DC converter

Figure 13 show the waveforms of primary voltages of three transformers. Each transformer primary voltage consists of three levels which include zero, 50V and -50V and each primary voltage of transformer are displaced with other two primary voltages of transformers by 120º. Figure 4.50 show the combined graph of all the primary voltages of the transformers.

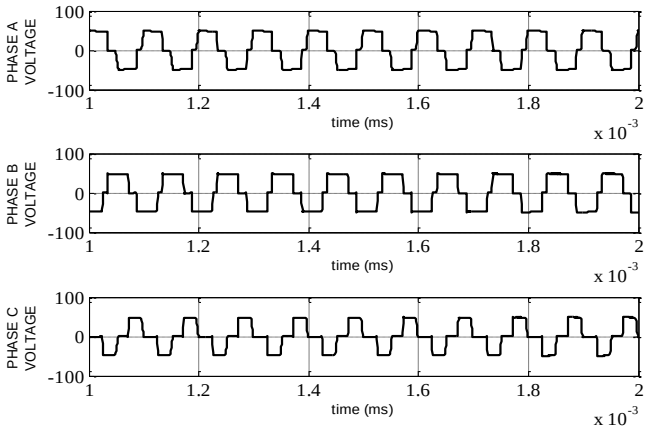

Figure 13: Three primary voltages of transformers

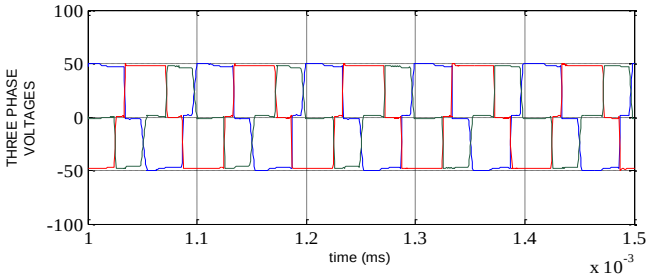

Figure 14: Three primary voltages of transformers combined in single graph

Figure 14 shows the dc output voltage waveform of the proposed converter with filter. The dc filter values are designed in a way that the maximum acceptable ripple content in dc output voltage and current is 3%. The dc output voltage is reached to its settling value at time t=0.015s.

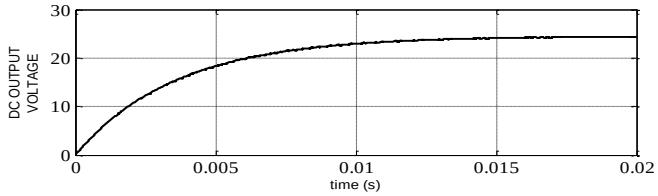

Figure 14: DC output voltage waveform with filter.

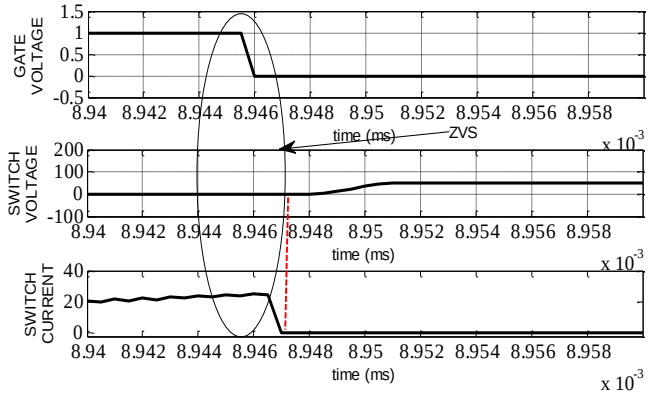

Figure 15: Gate voltage, voltage across and current through S_1 during ON to OFF

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Figure 15 and 16 show the gate voltage, voltage across and current through switch S_1 during on state to off state and off state to on state instants respectively. From Figure 15, during turn-off transition the collector to emitter voltage of switch is still zero due to its intrinsic capacitor C_1 but the collector current of S_1 starts falling. Thus, it can be noticed that the switch S_1 turns-off in ZVS mode. From Figure 16, the voltage across device once almost reached to zero, the gate to collector voltage is applied, thus indicates ZVS turn on action for switch S_1. Due to soft switching, there will be no voltage spikes in the primary side switches. The voltage stress in the primary side of switches becomes half of the input dc voltage, as a result the conduction losses are reduced and low rated devices can be used for high power applications.

Figure 17 show the gate voltage, voltage across and current through switch S_2 during on state to off state transition period. At time t=8.769ms, the switch S_2 is changing its state from on to off. The voltage across switch S_2 is still zero due to its intrinsic capacitor C_2. Hence this switch is operating under ZVS during on state to off state switching transition period.

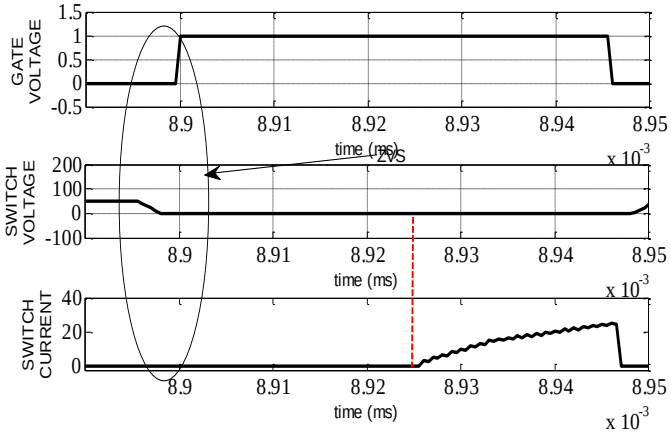

Figure 16: Gate voltage, voltage across and current through S_1 during OFF to ON

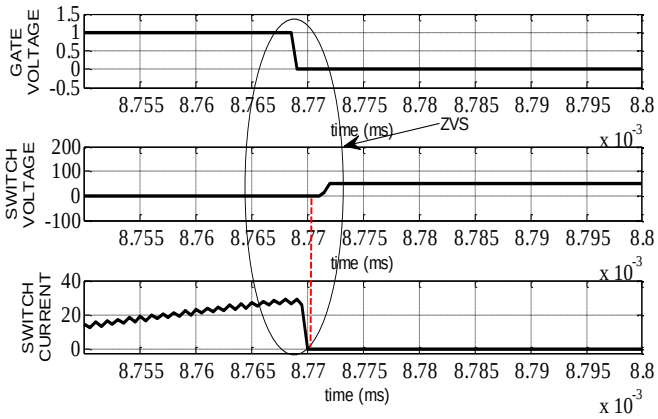

Figure 17: Gate voltage, voltage across and current through S_2 during ON to OFF

Figure 18 show the gate voltage, voltage across and current through switch S_2 during off state to on state transition instant. The switch S_2 is turned on at time t=8.735ms, the collector current of S_2 starts rising due to leakage & magnetizing inductances of transformer, whereas the collector-emitter voltage of S_2 is clamped to zero by the body diode of S_2. Hence, the switch S_2 is operating under ZVS during off state to on state transition period and no switching power loss in this transition instant. In the similar manner, the remaining control switches also operate under ZVS during switching transition period.

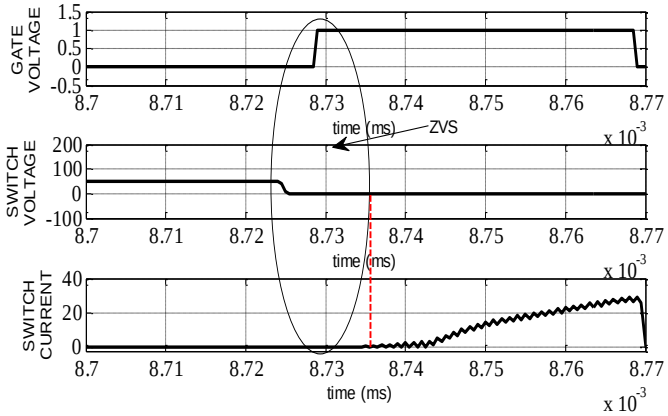

Figure 18: Gate voltage, voltage across and current through S_2 during OFF to ON

Table 3 shows the % efficiencies of the proposed three-phase three-level DC-DC converter for different load currents. The performance of proposed three-phase three-level DC-DC converter is compared with the existing three-phase three-level DC-DC converter [6] with same parameters as specified in table 4 in order to realize the proposed work. It is noticed that the efficiency of proposed three-phase three-level DC-DC converter was higher than the existing three-phase three-level DC-DC converter [6].

Table 3: Comparison of efficiencies proposed converter for various load currents

S.NO	LOAD CURRENT (Amps)	OUTPUT POWER (Watts)	INPUT POWER (Watts)	EFFICIENCY (%)
1	8.5	204.7	333.2	61.2
2	22	532.9	703.3	75.77
3	26	628.1	742.9	84.5
4	40	995	1111	89.6
5	54	1298	1417	91.63
6	60	1445	1558.7	92.7
7	72	1750	1854.4	94.37
8	78	1875	2083.3	90.1
9	80	1925	2182.5	88.2

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Table 4. Comparison of efficiency of proposed converter with existing converter for various load currents

S.NO	LOAD CURRENT (Amps)	% Efficiency	
		Proposed Three-phase three-level DC-DC converter	Existing three-phase three-level converter [6]
1	50	91.6	90.25
2	60	92.7	90.1
3	70	94.32	89.6
4	80	88.2	87

3. Conclusion

The proposed three-phase three-level isolated DC-DC converters have the advantages of soft switching and three-level voltage waveform in the primary side of transformer. The proposed three phase three level DC-DC converter based on the sequence of triggering the control switches and generates three level voltage waveform in the primary side of transformer to reduce the size of dc filter. Hence, the size of output dc filter reduced in 3-phase three-level DC-DC converter topologies. The size of leakage inductance of high frequency transformer was smaller for achieving soft switching. Hence, the cost and switching losses were reduced to a greater extent, thus improves the overall efficiency of a DC-DC converter. The efficiency of the proposed three-level isolated DC-DC converter was compared with the existing three-level DC-DC converter, from the comparison, it was cleared that the efficiency of the proposed three-level DC-DC converter was higher than the existing three-level DC-DC converter.

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