Single Input Single Output Two Level Isolated Dc-Dc Converter With Secondary Side Phase Shifting For Solar Applications

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Abstract: The isolated dc–dc converters with primary-side phase shifting (PPS) provides severely narrow soft-switching range for main devices in the primary side leg of full bridge converter. The leakage inductance of the high frequency transformer should be large enough for providing the energy needed for soft switching operations and also the idling power loss due to circulating current in the converter legs under large phase-shift angle, which makes reduction of conversion efficiency and complicated in designing the parameters of transformer. Furthermore, the turn-off diode commutations in the output-side rectifier are performed by hard-switching mode. To overcome all these drawbacks, a secondary side phase shifting (SPS) technique has been developed for two-level isolated DC-DC converter. This scheme provides wider soft switching range and reduced power loss due to elimination of circulating current in the primary side of high frequency transformer. In addition, SPS control also provide no reverse recovery current in diodes and hence no power losses in the secondary rectifier circuit. The control switches operate under soft switching even under rated load and short circuit conditions.

***Keywords*: *Single Input, Single output, Isolated* DC-DC Converter, Switching losses. Zero voltage Switching (ZVS), Secondary Side phase shifting (SPS)**

1. Introduction

In [1] &[2] several active snubbers and in [2]&[3] several passive snubbers , auxiliary and clamp circuits were proposed to resolve the issue concern the resetting of primary current of transformer to make ZCS of devices in the right leg of converter. The selected converters are very well adapted for no load and normal load, whereas at short circuit, they do not minimize freewheeling current and, therefore, turn-off and conduction losses occur. The clamp voltage is lower or equal than the output voltage, and thereby the commutation between the clamp and output rectifier is long, especially at high-current, high leakage inductance of the power transformer and low-output-voltage applications.

Several techniques have been developed to extend ZVS range to get better efficiency of full-bridge phase-shift controlled converters, [4]–[7].

A primary-side phase shifting is a typical and basic control scheme has been developed in [8], [9], this technique reduces electromagnetic interference. In addition, the pulse width modulation (PWM) zero-voltage switching dc–dc converters with primary-side phase shifting have a severely narrow soft-switching range for main devices in the PS leg of FB inverter. The leakage inductance of the HF transformer should be large enough for providing the energy needed for soft switching operations, which makes reduction of conversion efficiency and complicated in designing the parameters of transformer. The idling power loss due to circulating current in the inverter legs under large phase-shift angle. This result, the converter efficiency of dc–dc converters severely decreases, in especially, for the light load power ratings [17] and [18]. Furthermore, the turn-off diode commutations in the output-side rectifier are performed by hard-switching mode, which operates with the voltage surges and thereby reduction of converter efficiency.

To overcome the limitations of PWM- ZVS dc–dc converters, secondary-side phase shifting has been considered and the related soft-switching dc– dc PWM converter circuits have been introduced for generation of power supplies. The first time secondary-side phase shifting scheme was introduced in [10], here the saturable inductors are used as the primary side-controlled devices. Even though some challenges still present, the PWM dc–dc secondary side phase shifting controlled converters are attractive because of simple structures and wide range of soft-switching operations. The effectiveness of secondary-side phase shifting schemes with active rectifiers is discussed over the past few years while number of other technical papers has discussed the PWM dc–dc converters with primary side phase control. In [11], the idea of secondary side phase shifting scheme for a PWM ZVS dc–dc converter, and indicated the fundamental principle along with theoretical analyses and fundamental experimental discussions are presented. The discussions and practical evaluations on voltage regulations and output power as well as the conversion efficiencies under the different load conditions are unclear. The secondary-side phase-shift control mechanism

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is proposed in [12]-[14], where the duty cycle of both secondary and primary active devices keeps 0.5 and the phase-shift angle between secondary and primary devices is selected as the freedom to control and regulate the output voltage.

In this research work, a secondary side phase shifting mechanism has been proposed. With the proposed secondary-side phase shifting control scheme, the freewheeling current is effectively eliminated and the voltage spikes on secondary-side devices are suppressed. The soft-switching dc–dc converters with secondary-side phase shift can provide wide range of soft-switching conditions and effective minimization of power loss drawing from the circulating current in the primary-side of high frequency transformer. In addition, the secondary-side phase shifting PWM ZVS dc–dc converter is free with diode reverse recovery current and related power loss in the output side of rectifier, so, the RCD snubbers for rectifying diodes are eliminated.

The paper is divided into three sections. The introduction of paper is given in section 1. The modes of operation, realization of soft switching, design equations, and results of proposed single input single output two-level DC-DC converter with SPS are presented in section 2 and 3. The conclusion of the paper is given in section 4.

2. ZVS ISOLATED DC-DC CONVERTER WITH SECONDARY SIDE PHASE SHIFTING:

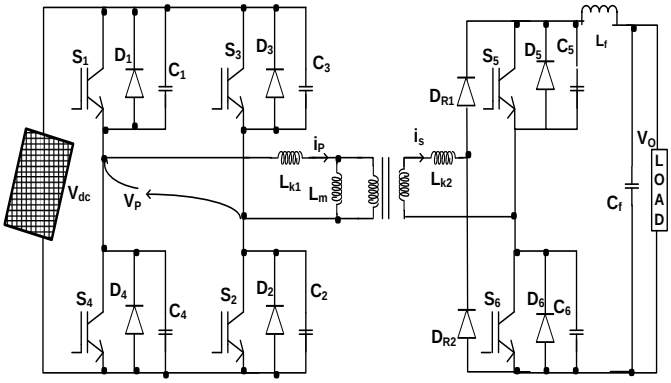

Figure 2.1: ZVS-PWM dc–dc converter with SPS active rectifier.

The figure 2.1 shows the circuit diagram of two level single input single output ZVS isolated DC-DC converter with secondary side phase shifting. The switches S_1-S_4 are the transformer primary switches and S_5 & S_6 are the bidirectional transformer secondary switches. The switches S_5 and S_6 operate in the phase shift manner with the primary side switches S_1 and S_3. The switches S_1 and S_3 are turned on complementarily for 180° period.

The advantages of SPS scheme are:

(i) Wider soft switching range is possible due to load variations

(ii) No idling power loss due to circulating current in the primary side

(iii) No additional components are required for achieving soft switching

(iv) The secondary side diodes are operating under ZVS for turn on/off transitions. So, the reverse recovery current in diode is eliminated.

(v) The dynamic response of a converter is faster due to load variations because of presence of secondary control scheme.

Modes of operation:

The figure 2.2 shows the operational waveforms of proposed converter. The figures 2.3 to 2.12 show the modes of operation of two level ZVS DC-DC converter with SPS for one cycle.

Mode 1 ($t_0 \leq t < t_1$):

During this mode, the switches S_3 and S_4 are turned off under ZVS. So, the capacitors C_3 and C_4 are starts charging whereas capacitors C_1 and C_2 are discharging through the current in primary winding of transformer. The switch S_5 is still on along with diode D_5 and D_{R2} and majority of the current is transmitted through D_5 and D_{R2} only, as shown in figure 2.3. The capacitors C_1 and C_2 are fully discharged to zero before time $t=t_1$. Hence its body diodes D_1 and D_2 are on. So, the switches S_1 and S_2 are ready to operate under ZVS at the end of time $t=t_1$.

The voltage across switches S_1-S_4 under this mode are,

$$v_{C1}(t)=v_{C2}(t) = I_p . Z_1 . \sin [w_1(t - t_0)] \quad (2.1)$$

$$v_{C3}(t)=v_{C4}(t) = V_{dc} - I_P . Z_1 . \sin [w_1(t - t_0)] \quad (2.2)$$

Where I_p represents the transformer primary current at $t=t_0$, t_5, t_{10} in figure 2.2. Where $Z_1 = \frac{1}{W C_1} = \frac{1}{2\pi f_s C_{r1}}$, $\omega_1 = \frac{1}{2L_{kp}C_{r1}}$, $C_1 = C_{r1} = C_2 = C_3 = C_4$, L_{kp} indicates the inductance referred to primary side of converter, L_m is the magnetizing inductance and ω_1 is the primary side angular resonant frequency.

$$L_{kp} = L_{k1} + N_T^2 L_{k2} \ll L_m \quad (2.3)$$

Mode 2 ($t_1 \leq t < t_2$):

At time $t=t_1$, the switches S_1 and S_2 are turned on under ZVS. Due to leakage inductances in the transformer primary and secondary, the primary current is still not reached to zero. In this mode, the switch S_5 is still on along with D_5 and D_{R2} in the secondary side of transformer, as shown in figure 2.4.

The value of primary current from mode 1 to mode 2 is

$$i_p(t) = \frac{V_{dc}+N_T V_0}{L_{kp}} (t - t_0). \quad (2.5)$$

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Where N_T ($=N_P/N_S$) indicates turn ratio of transformer from primary to secondary.

The transition period T_{c1} for the switches S_1–S_4 can be determined from equations (2.1) and (2.2) for ZVS commutation as

$$T_{c1} = \frac{1}{W_1} \sin^{-1} \left(\frac{V_{dc}}{Z_1 I_p}\right) \leq t_{0-1} \quad (2.4)$$

Where t_{0-1} denotes the dead time of the switches S_1/S_4 and S_3/S_2.

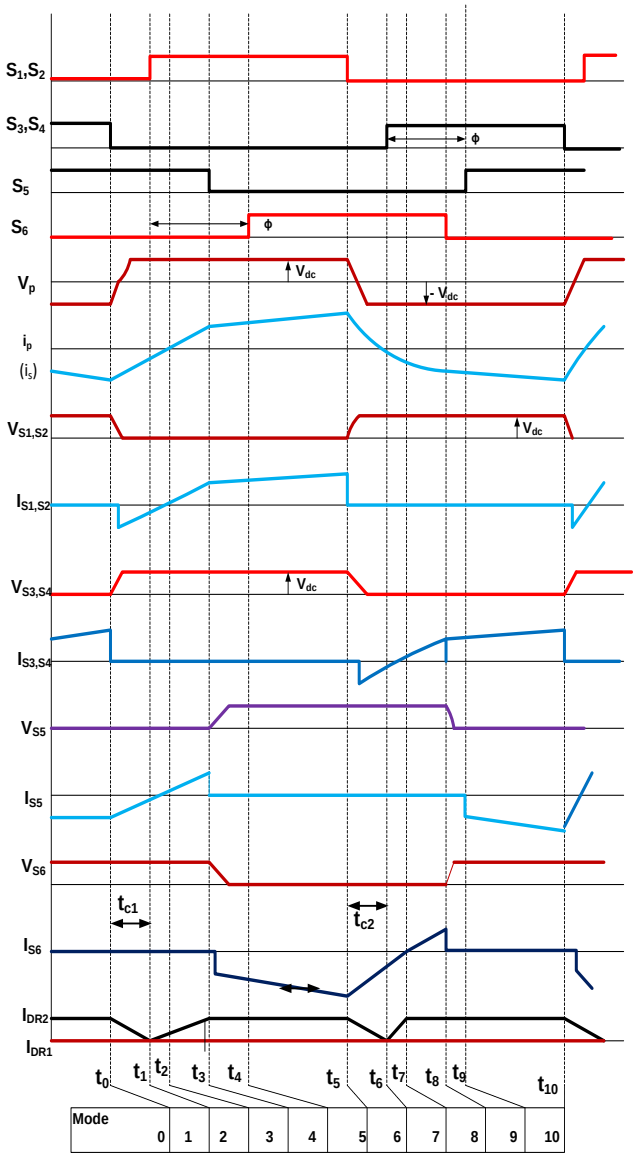

Figure 2.2: Relevant voltage and current waveforms of proposed DC-DC converter

Mode 3 ($t_2 \leq t < t_3$):

At time $t=t_2$, the primary current in the circuit is reached to zero from negative direction and thereby the diode D_{R2} is turned off due to reversed biased condition and D_{R1} is turned on along with conducting switch S_5 due to forward biased condition. Here, the diode D_{R2} is off under ZCS and D_{R1} is on under ZCS. In this case, the load is disconnected from the dc source and it is indicated in figure 2.5.

The current i_p in this mode is,

$$I_p(t) = \frac{V_{dc}}{L_{kp}}(t - t_0) \quad (2.6)$$

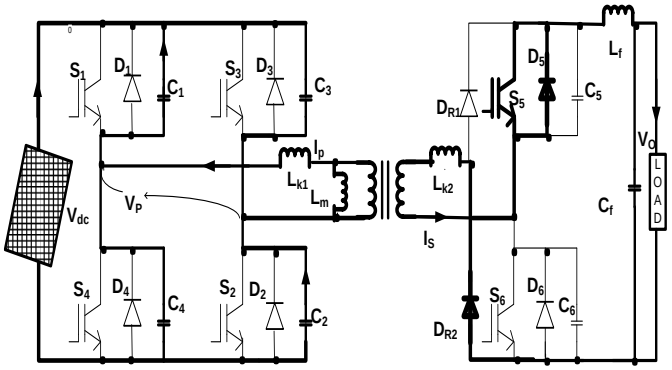

Figure 2.3: Equivalent circuit for mode '1' operation

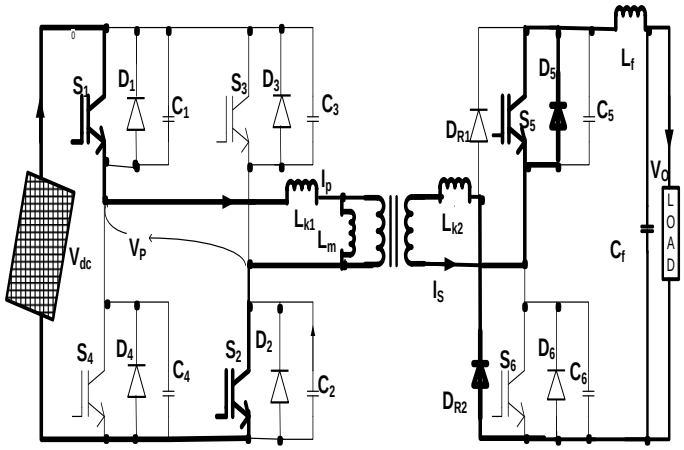

Figure 2.4: Equivalent circuit for mode '2' operation

Mode 4 ($t_3 \leq t < t_4$):

At time $t=t_3$, the switch S_5 is turned off under ZVS. So, the capacitor C_5 starts charging where as capacitor C_6 starts discharging based on the direction of current in the secondary side of transformer. The primary side switches S_1 and S_2 are still on and the load receives power from source through secondary diode diode D_{R1} as indicated in figure 2.6. The capacitor C_6 is completely discharged to zero before time $t=t_4$. Hence, the body diode of switch S_6 is on and thereby the switch S_6 is ready to operate under ZVS at the end of time $t=t_4$.

The S_5 and S_6 switch voltages are

$$v_{C5}(t) = I_s . Z_2 . \sin [w_2(t - t_3)] \quad (2.7)$$

$$v_{C6}(t) = V_o - I_s . Z_2 . \sin [w_2(t - t_3)] \quad (2.8)$$

Where I_s represents the transformer secondary current. Where $Z_2 = \frac{1}{WC_{r2}} = \frac{1}{2\pi f_s C_{r2}}$, $\omega_2 = \frac{1}{2L_{ks}C_{r2}}$, $C_5 = C_{r2} = C_6$, L_{ks} indicates the inductances referred to secondary as,

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$$L_{ks} = L_{k2} + \frac{1}{N_T^2} L_{k1} \ll L_m \qquad (2.9)$$

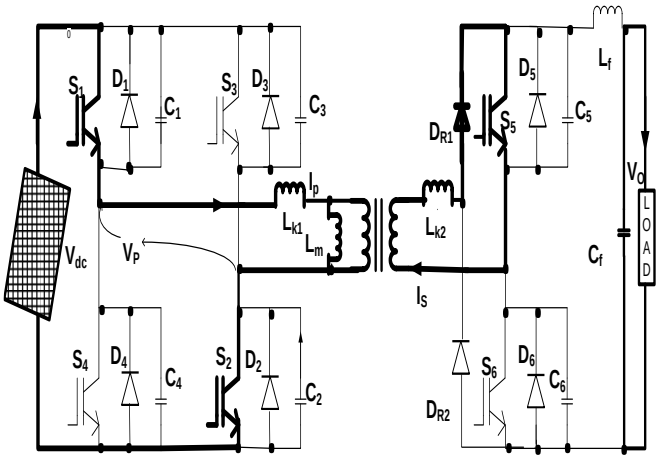

Figure 2.5: Equivalent circuit for mode '3' operation

The transition period T_{c2} for the switches S_5 and S_6 can be determined from equations (2.7) and (2.8) for ZVS commutation as

$$T_{c2} = \frac{1}{w_2} \sin^{-1}\left(\frac{V_0}{Z_2 I_s}\right) \leq t_{5-6} \qquad (2.10)$$

Where t_{5-6} indicates the dead time for the switches S_5 and S_6.

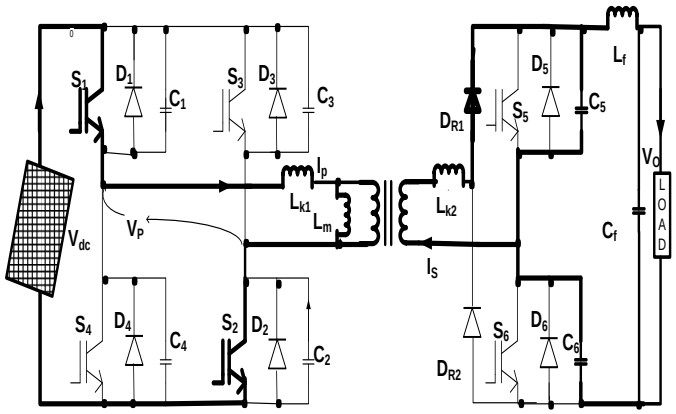

Figure 2.6: Equivalent circuit for mode '4' operation

Mode 5 ($t_4 \leq t < t_5$) :

At time $t=t_4$, the control switch S_6 is on under ZVS along with the conducting diode D_{R1} in the secondary side. The current in the circuit is flowing from zero to positive direction and load receives power from dc source through switches S_6 and D_{R1}, as shown in figure 2.7.

The current expression from mode 4 to mode 5 is

$$i_p(t) = \frac{V_{dc} - N_T V_0}{L_{kp}} (t - t_5) \qquad (2.11)$$

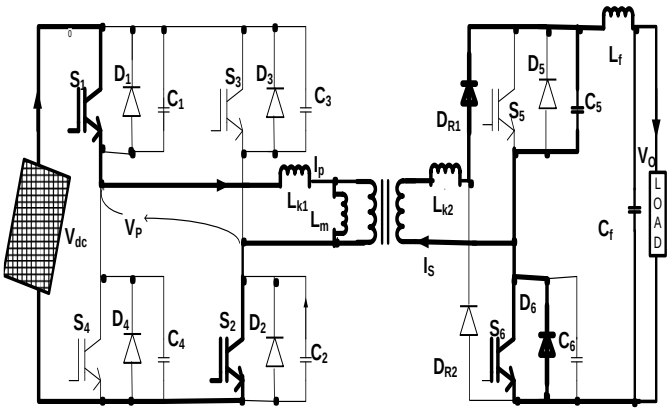

Figure 2.7: Equivalent circuit for mode '5' operation

Mode 6 ($t_5 \leq t < t_6$):

At time $t=t_5$, the switches S_1 and S_4 are turned off under ZVS. So, the capacitors C_1 and C_2 are starts charging and capacitors C_3 and C_4 are starts discharging through current in the primary side of transformer. The idling power loss due to circulating current in the primary side can be reduced due to phase shift control switch S_6. The switch S_6, diodes D_6 and D_{R1} are operating in the secondary side and majority of the current flows through the diodes D_6 and D_{R1} only. Before time $t=t_6$, the capacitors C_3 and C_4 are completely discharged to zero. Hence the body diodes of switches S_3 and S_4 are on and thereby the switches S_3 and S_4 are ready to operate under ZVS at the end of time $t=t_6$, as shown in figure 2.8.

Mode 7 ($t_6 \leq t < t_7$):

At time $t=t_6$, the switches S_3 and S_4 are turned on under ZVS. Due to leakage inductances in the transformer, the current in the circuit cannot change suddenly from positive to negative. Therefore the diode D_{R1} is still on along with control switch S_6 and D_{R2} in the secondary side, as shown in figure 2.9.

Mode 8 ($t_7 \leq t < t_8$):

At time $t=t_7$, the current in the circuit is changed from positive to zero. Hence the diode D_{R1} is off under ZCS due to reversed biased condition and diode D_{R2} is on under ZCS due to forward biased condition with the conducting switch S_6. In this mode, the load is disconnected from the dc source and it is shown in figure 2.10.

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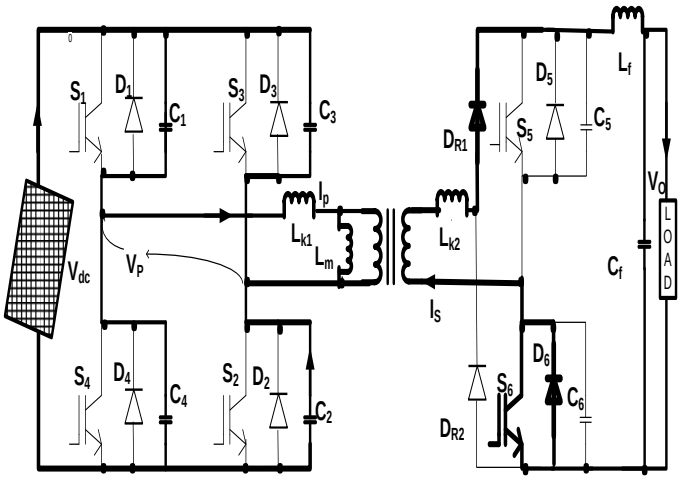

Figure 2.8: Equivalent circuit for mode '6' operation

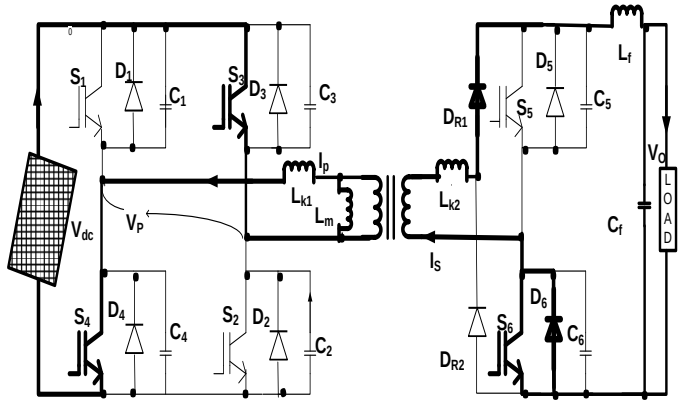

Figure 2.9: Equivalent circuit for mode '7' operation

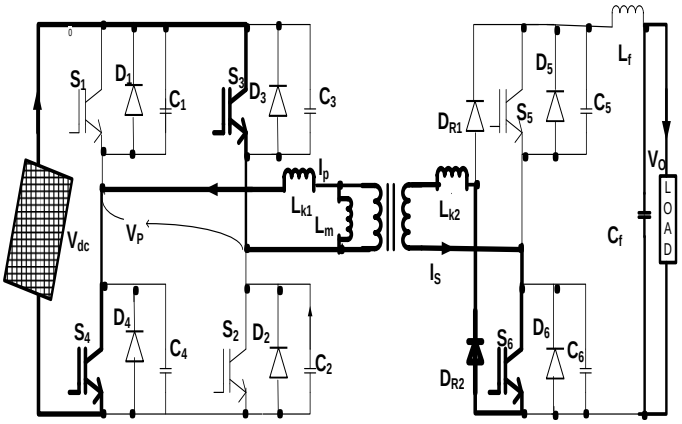

Figure 2.10: Equivalent circuit for mode '8' operation

Mode 9 ($t_8 \leq t < t_9$):

At time $t=t_8$, the switch S_6 is turned off under ZVS. The capacitor C_6 starts charging whereas the capacitor C_5 starts discharging. The load receives power from source through the diode D_{R2} in the secondary side and the switches S_3 and S_4 in the primary side. Before time $t=t_9$, the capacitor C_5 is fully discharged to zero and corresponding body diode of S_5 is on. Therefore the switch S_5 is ready to operate under ZVS after time $t=t_9$, as shown in figure 2.11.

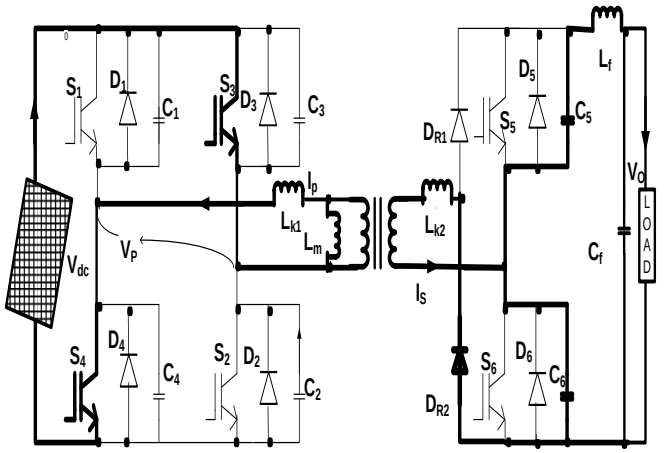

Figure 2.11: Equivalent circuit for mode '9' operation

Mode 10 ($t_9 \leq t < t_{10}$):

At time $t=t_9$, the switch S_5 is on under ZVS along with the conducting diode D_{R2}. So, the current in the circuit is flowing from zero to negative direction through the primary switches S_3 and S_4 and the secondary side switches D_{R2} and S_5 as shown in figure 2.12.

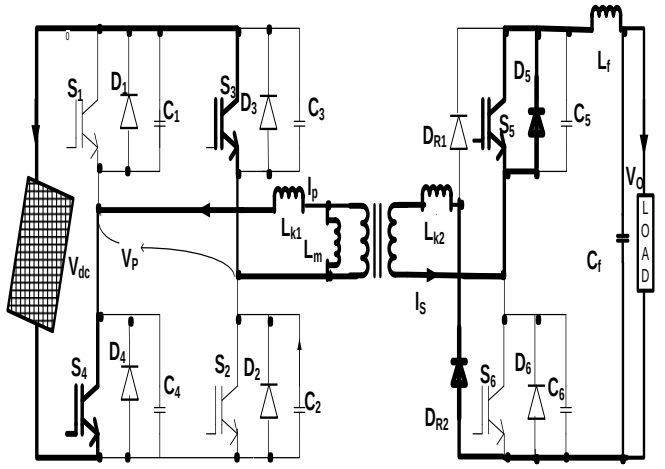

Figure 2.12: Equivalent circuit for mode '10' operation

2.2.1 Realization of soft switching:

As compared to primary side phase shifting scheme, the secondary side phase shifting scheme can reduce the circulating current in the primary side of inverter. Due to this feature, the soft switching is simple and wider.

The primary voltage and current waveform of primary side of inverter in PPS and SPS schemes are shown in figures 2.13 (a) and (b). The edge resonance in the lagging phase shift switches S_2 and S_3 are depends on the magnitude of circulating current. The ZVS operation is not possible in the phase shifted switches S_3 and S_2 during low output power. The SPS scheme does not provide any lagging phase shift in the

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primary side of inverter. Hence all the control switches in the primary side of transformer are under ZVS, hence

$$\frac{L_{kp}^2 * I_p^2}{2} > 2 * V_{dc}^2 * C_{r1} \quad (2.12)$$

I_p denotes the magnitude of primary current and $C_1=C_2=C_3=C_4=C_{r1}$ is the primary resonant capacitor.

In addition to (2.12), the equation (2.4) must be satisfied in the ZVS condition in the secondary side switches S_5 and S_6 are

$$\frac{L_{kp}^2 * I_s^2}{2} > \frac{C_{r2} * V_{dc}^2}{N_T^2} \quad (2.13)$$

I_s denotes the magnitude of secondary current and $C_5=C_6=C_{r2}$ is the secondary resonant capacitor.

In addition to equation (2.13), the equation (2.10) must be satisfied in this case. The equations (2.12) - (2.13) and (2.4) - (2.10) shows that the soft switching range in the proposed converter depends on the load power. The soft switching is very critical in the light load conditions. In order to achieve wide range of ZVS in the light load conditions, an introduction of dead time control to SPS scheme is to be added.

The rectifying diodes D_{R1} and D_{R2} are turned-off under ZCS. These switches are operating under ZCS in the full load range. There are no parasitic ringing in ZCS turn-off commutating diodes D_{R1} and D_{R2}. Hence no active and passive snubber for voltage clamping in the rectifying diodes are required. Therefore the switching power losses and conduction losses can be minimized in the secondary diodes D_{R1} and D_{R2}.

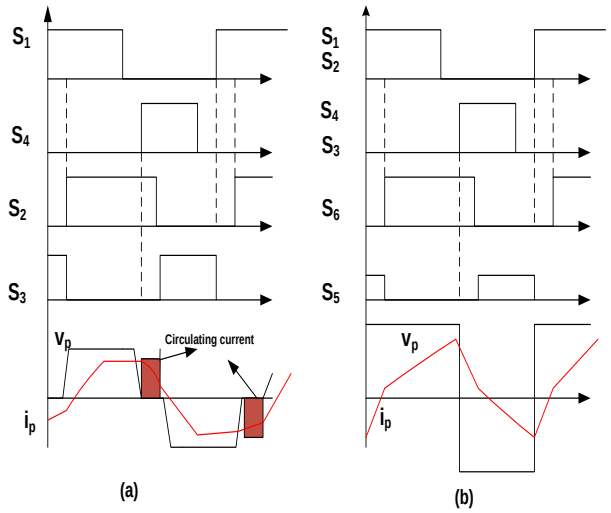

Figure 2.13: Phase shifting gate pulse patterns and waveforms in primary-side inverter: (a) PPS (b) SPS.

2.2.3 Design equations:

The converter design indicates the design of values for C_1, C_2, C_3, C_4, C_5, C_6, L_{k1}, L_{k2}, L_f and C_f.

The output inductor should be large enough to make the output current should be continuous throughout the switching period and leakage inductance of transformer must be small enough to make the less reset time.

The resonant capacitor C_{r1} ($=C_1=C_2=C_3=C_4$) must be selected in such a way that the minimum requirement for ZVS operation of control switch during turn-off. The large capacitance is required to hold the switch voltage closed to zero during current fall time of the switch (t_{fi}). The value of t_{fi} can be taken from the data sheet. The value of C_{r1} can be calculated as,

$$C_{r2} = \frac{t_{fi} * I_s}{V_o} \quad (2.15)$$

The resonant capacitor C_{r2} ($=C_5=C_6$) must be selected in such a way that the minimum requirement for ZVS operation of control switch during turn-off. The large capacitance is required to hold the switch voltage closed to zero during current fall time of the switch (t_{fi}). The value of C_{r2} can be calculated as,

$$C_{r2} = \frac{t_{fi} * I_s}{V_o} \quad (2.15)$$

The dc output filter elements are designed based on the following equations:

$$\Delta I_o = \frac{V_o * (1-k) * T_s}{L_f} \quad (2.16)$$

$$\frac{\Delta V_o}{V_o} = \frac{\pi^2 * (1-k) * f_r^2}{f_{sw}^2} \quad (2.17)$$

$$f_r = \frac{1}{2 * \pi * \sqrt{L_f * C_f}} \quad (2.18)$$

Where ΔV_o & ΔI_o are the acceptable ripple contents in the dc output voltage and current waveforms, V_o is the required dc output voltage, f_r is the resonant frequency, $f_{sw}=(1/T_s)$ is the switching frequency and k is the duty cycle of switch.

3. Results and Discussions:

The parameters of the proposed converter circuit shown in figure 2.1, are given in table 2.1

Table 2.1: Converter parameters

Name of the parameter	Value
Switching frequency, f_{sw}	10KHz
DC Input voltage, V_{dc}	100V
DC Output voltage, V_o	24V
Parasitic capacitor, C_r	0.01PF
Leakage Inductance of transformer, L_{lk}	4.86uH
Magnetizing Inductance of transformer, L_m	3.97H

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Turns ratio of transformer (N_P:N_S), N_T	4:1
DC filter inductance, L_f	65mH
DC filter capacitance, C_f	50uF
DC load current, I_o	40A
Power Rating, P	1000W

Figure 2.14 show the gate pulses of the proposed converter switches. Sufficient dead time (t_{dead}) is created between the control switches S_1&S_4, S_3&S_2 and S_5&S_6 to avoid the source short circuit problem. The dead time is calculated based on the following equation

$$t_{dead} = C_r * \frac{V_{dc}}{I_{p0,min}} \qquad (2.19)$$

Figure 2.15 show the voltage and current waveforms of transformer primary. From the figure, it is observed that the primary current of transformer increases gradually due to presence of leakage inductance and magnetizing inductance of the transformer which causes increase of the range of ZVS condition for primary side converter switches. When the positive V_{dc} appears across the primary of the transformer, the current which is passing through the primary is of 5A magnitude. Similarly, when the negative V_{dc} appears across the primary of the transformer, then the reversed current flows through the primary of the transformer which is of 5A magnitude.

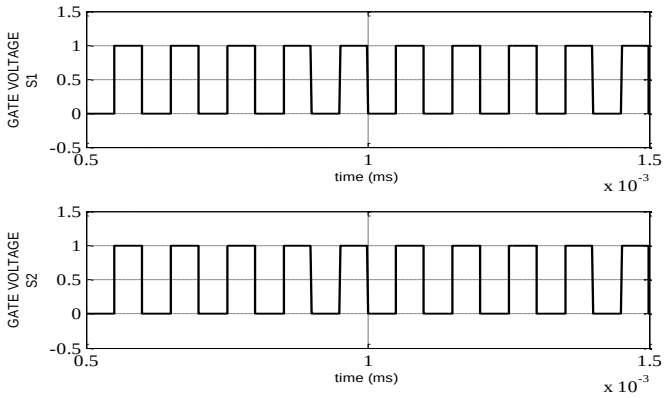

Figure 2.14 (a): Gate pulses for S_1 and S_2 switches

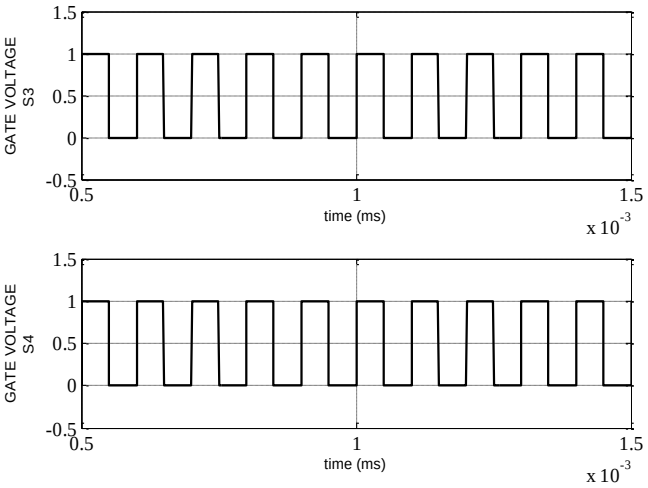

Figure 2.14 (b): Gate pulses for S_3 and S_4 switches

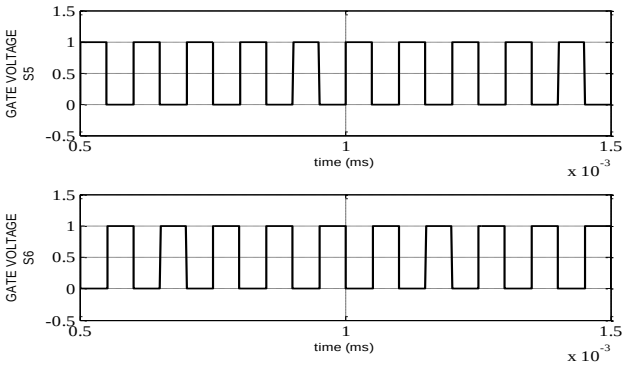

Figure 2.14 (c): Gate pulses for S_5 and S_6 switches

Figure 2.14: Gate pulses for proposed converter switches

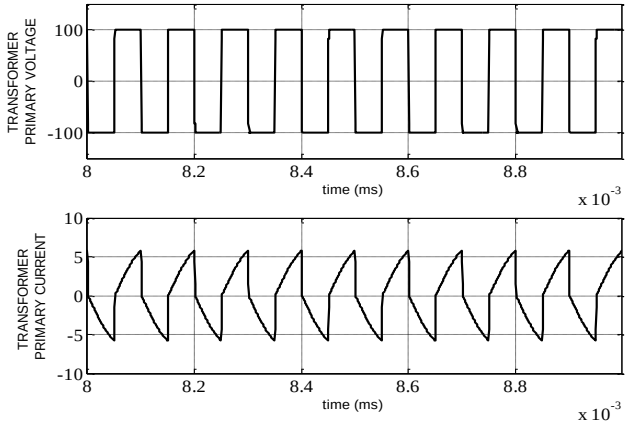

Figure 2.15 Transformer primary voltage and current waveforms

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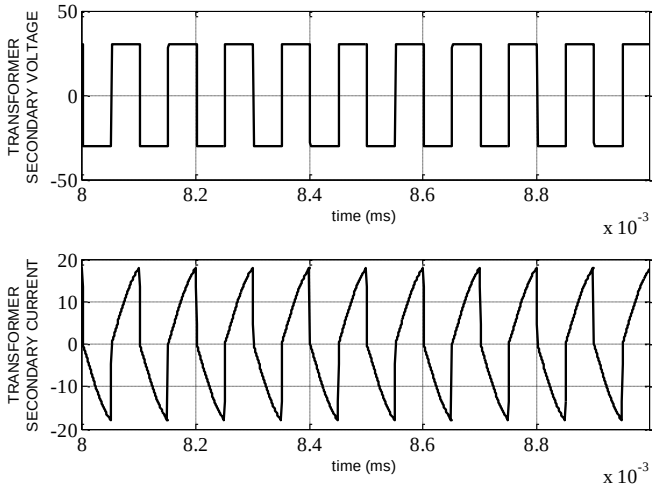

Figure 2.16: Transformer secondary voltage and current waveforms

Figure 2.16 show the voltage and current waveforms of transformer secondary. From the figure, it is observed that the secondary current of transformer increases gradually due to secondary leakage inductance of the transformer. When the positive $V_{dc}/4$ appears across the secondary of the transformer, the current which is passing through the secondary is of 18A magnitude and similarly the same thing happens for negative half cycle.

Figure 2.17 shows the dc output voltage waveform of the proposed converter with filter. The dc filter values are designed such a way that the ripple content present in dc output voltage and current waveform become less than 3%. From the figure it is noticed that the dc output voltage is reached to its steady state value at time t=2.5ms.

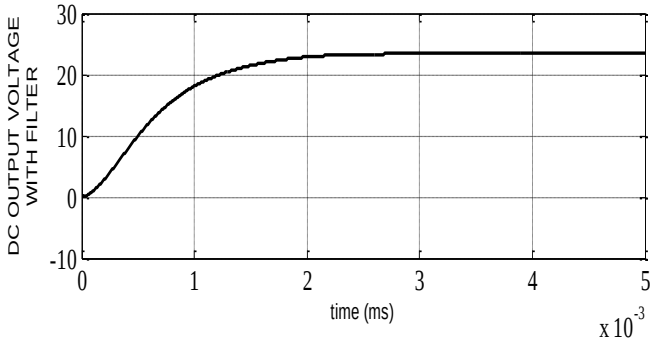

Figure 2.17: DC output voltage waveform with filter.

Figure 2.18 shows gate voltage, voltage across and current through switches S_1 & S_2 for the switching transition period from off state to on state. When the gate pulses are applied to S_1 & S_2, then the switches S_1&S_2 are turned on and current passes through the switch from time t=5.052ms, it is observed that the voltage across switch is still zero but current starts increasing, it indicates that the switching power loss is zero during transition period from off state to on state. That means ZVS is achieved for S_1 & S_2.

The ZVS is achieved across S_1 & S_2 due to clamping of the voltage to zero by the body diodes of S_1&S_2. Hence, the switches S_1&S_2 are turning on under ZVS during off to on transition period. The switches are completely turned on at time t=5.052ms, then the collector current of S_1&S_2 are starts rising from zero to 5A and the collector to emitter voltage of S_1&S_2 are decreased to zero due to their intrinsic capacitors C_1&C_2.

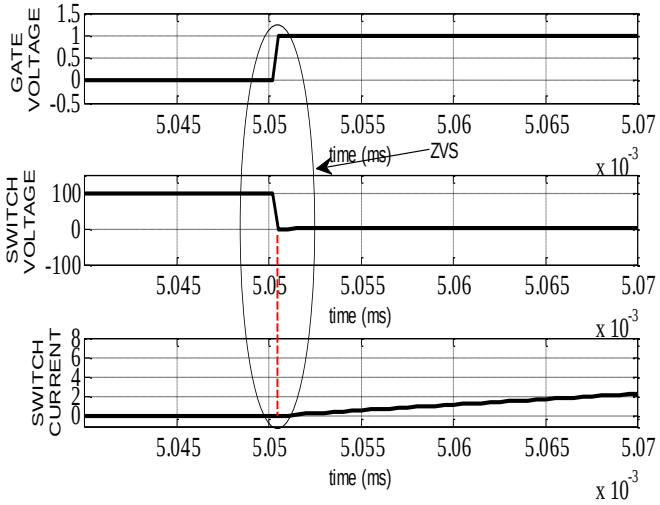

Figure 2.18: Gate voltage, voltage across and current through switches S_1 & S_2 during OFF to ON

Figure 2.19 shows the gate voltage, voltage across and current through switches S_1&S_2 during on to off transition period. From figure 2.19, the turn on to turn off transition of switches S_1&S_2 is occurred from the time 5.1ms to 5.1005ms. The collector current of S_1&S_2 starts falling from 5A to zero in this interval, where as the collector-emitter voltages of S_1&S_2 are clamped to zero due to their intrinsic capacitors C_1&C_2. Therefore, the switches S_1&S_2 are operate under ZVS during on to off transition instant and no switching power losses in this instant.

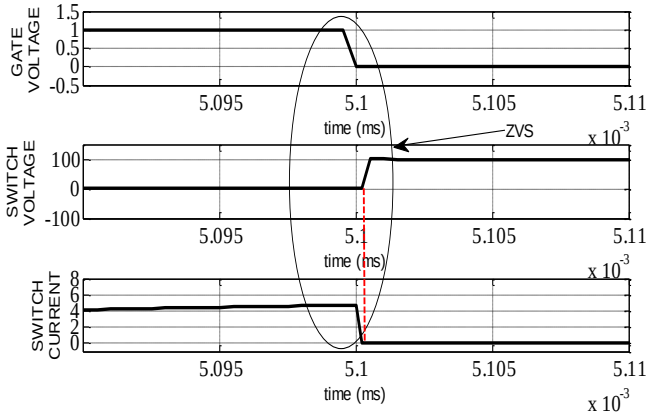

Figure 2.19: Gate voltage, voltage across and current through switches S_1 & S_2 during ON to OFF

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Figure 2.20 shows the gate voltage, voltage across and current through switches S_3 & S_4 during off to on transition instant. The switches S_3&S_4 have been achieved zero -voltage turn-on, since the voltage is reduced to zero before the device is switched, as shown in Figure 2.20. The ZVS of switches S_3&S_4 during turn-off is shown in Figure 2.21, here, the ZVS turn-off is achieved since the voltage across the switches rises during turn-off and reached to zero before the device finishes turning off. Hence, zero switching power loss during on state to off state and off state to on state transition instants.

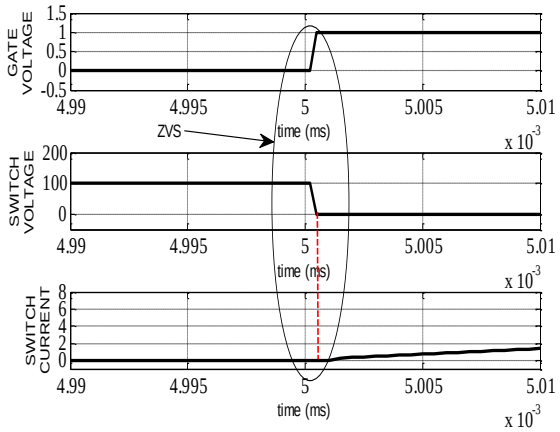

Figure 2.20: Gate voltage, voltage across and current through switches S_3 & S_4 during OFF to ON

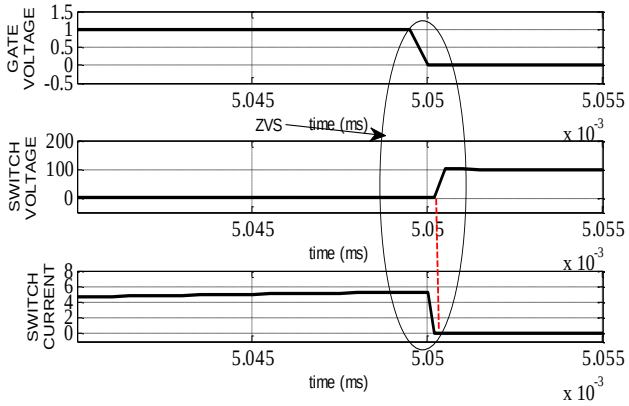

Figure 2.21: Gate voltage, voltage across and current through switches S_3 & S_4 during ON to OFF

Figure 2.22 and 2.23 show the gate voltage, voltage across and current through switch S_5 during turning off and turning on transition instants respectively. From figure 2.22, during turn on transition, the collector to emitter voltage of switch is reached to zero before collector current of switch rises from zero due to clamping of its body diode. Thus, it can be noticed that the switch S_5 turns-on under ZVS mode. From Figure 2.23, during turn-off transition, the collector to emitter voltage of switch has reached to zero before collector current of switch falls to zero due to its intrinsic capacitor C_5. Thus, it can be noticed that the switch S_5 turns-off under ZVS mode. Therefore, zero switching power loss during off state to on state and vice versa.

From figures 2.22 and 2.23, it shows that the voltage stresses on the secondary side are clamped to the output voltage and the voltage spikes on the secondary side are suppressed due to soft switching. In addition, there is no reverse recovery current in the rectifier diodes, because the rate of current falling is controlled by the transformer leakage inductance. In the similar manner, the control switch S_6 also operates under ZVS during switching transition period.

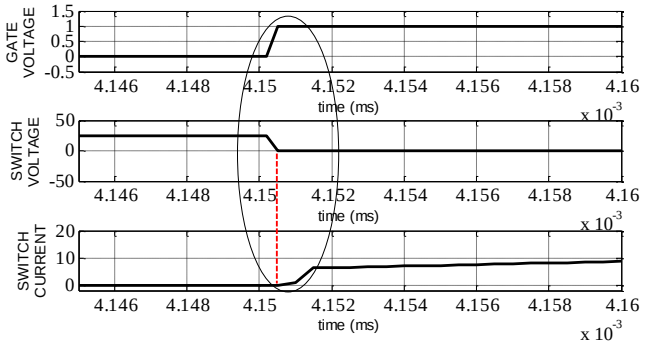

Figure 2.22: Gate voltage, voltage across and current through S_5 during OFF to ON

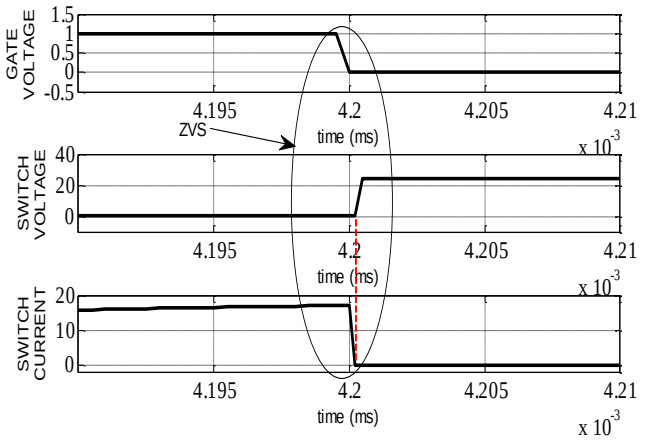

Figure 2.23: Gate voltage, voltage across and current through S_5 during ON to OFF

Table 2.2: Comparison of efficiencies of proposed converter for various load currents

S.NO	LOAD CURRENT (Amps)	OUTPUT POWER (Watts)	INPUT POWER (Watts)	EFFICIENCY (%)
1	6	159.1	186.1	85.5
2	12	299.4	335.7	89.18
3	16	424	472	89.86
4	22	541.1	602.3	89.85
5	31	763	884.9	86.26
6	34	814.8	958	85.05
7	38	902.7	1087	83.04
8	40	951.7	1174	81.09

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Table 2.2 shows the % efficiency of the proposed single input single output two level DC-DC converter with SPS for different load currents. Table 2.3 shows the % efficiency of proposed two level DC-DC converter with existing two level DC-DC converter [11] for various load currents. The performance of proposed two-level DC-DC converter is compared with the existing two-level DC-DC converter with same parameters as specified in table 2.1 in order to validate the proposed work. It is clear that the efficiency of proposed two-level SPS DC-DC converter is higher than the existing two-level DC-DC converter [11].

Table 2.3: Comparison of efficiency of proposed converter with existing converter for various load currents

S.NO	Load Current (Amps)	% Efficiency	
		Proposed Two-level SPS DC-DC Converter	Existing two-level DC-DC converter [11]
1	6	85.5	81.2
2	12	89.18	84.9
3	16	89.86	85.8
4	22	89.85	86.2
5	31	86.26	85.3
6	34	85.05	83.9

4. Conclusion

In this paper, soft switching control strategy for single input single output two-level isolated DC-DC converter with secondary side phase shifting (SPS) was developed. The proposed converter with SPS was provided wider soft switching range and reduced power loss due to reduction of circulating current in the primary side of high frequency transformer. In addition, the proposed scheme provide no reverse recovery current in diodes and hence no power losses in the secondary side rectifier circuit. The efficiency of the proposed two-level DC-DC SPS converter was compared with existing two-level DC-DC converter for validating the proposed work. From the comparison, it was noticed that the efficiency of the proposed DC-DC converter with SPS is higher than the existing two-level DC-DC converter.

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