HDL Implementation of Scalable Architecture for Packet Classification using Field Split Bit Vector Algorithm

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Abstract: **The categorization of incoming packets can be considered as a classification based on the fields of the different headers, such as the source-Internet protocol, the target-Internet protocol, the source-port, destination-port and protocol fields. It requires that each packet is compared with rules and each packet is forwarded to the highest priority matching rule. Packet classification performance also depends on the rule sets. The required storage depends generally on the number of rules and the size of the method. In this paper, we described a Modular Field Split Bit-Vector (FSBV) algorithm, with which the Field Programmable Gate Array (FPGA) classification of packets is performed using Xilinx ISE13.1 software, with a few predefined rules. From the results obtained through EDA tools, it can be concluded that the proposed technique is memory-efficient and latency aware.**

Keywords: Field Split Bit Vector Algorithm, Packet Classification 5-tuple, Latency, Throughput, Bit Vector Algorithm, Latency.

1. Introduction

Packet is the data unit routed on the Internet or any other packet network between the source and the destination. If any file is sent on the internet from place to place, The TCP/IP layer divides the file into an efficient routing chunk. Individual packets can use the internet on different routes. They are all in the original file when they arrive. Classification of the PACKET is a technique used for different purposes for networking equipment [1]. Each rule is made up of several sub-rules that regulate the headers. The bit width of the sub-regulator gives the user the option to control, which decides the architectural performance. We are further enhancing our approach's scalability by increasing our memory efficiency and throughput which is measurable in terms of latency, memory and a pipeline system. When the highest-weighted rule is matched, the output of the algorithm is also known as the match number. The demand for higher packet bandwidth is increasing at the same time that the networks are becoming faster You should not try to rush wire processing in order to achieve constant time. Although rule processing often creates a fast data structure that supports rule processing, it does not have to be that way [2]. The algorithm presented in this paper uses fast match, consumes less memory [3], and has fewer header fields. In future high-speed networks, the speed detection is not fast enough to meet requirements, so future applications will extract and process packets rather than transmit them. Classifying packets according to their value produces greater profits. There are various network services, such as guided routing, quality routing, private virtual networking, available to assist with addressing complex issues on your company may have. In theory, the header database has different rules for each packet type. Processing speed is dependent on two factors: computation speed and operating speed. Without meeting the processing speed minimum requirements [4], the router may be able to handle real-time video applications The second reason is that a buffer overflow may or may cause the router to not to drop packets. With respect to classifying packets, processing speed is most important. One of the most important time-

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consuming tasks in a packet classification algorithm is the use of memory accesses. In the first stages of the Internet, most of the rules were put in place to limit the flow of information, such as the firewall and the database. For more rule databases to be created, the Internet will have to grow. Routers determine how packets should be classified according to the IP headers. It differs from the averaged bit vector algorithm by having less redundant bits. The critical part of this article presents an HDL (acronym for "high-level synthesis language") packet classification for FPGA. Since PEs are designed to be self-configurable, and fast processing is essential, they can process a lot of different kinds of information. This helps the network keep its top-notch performance.

2. Algorithms for Packet categorization

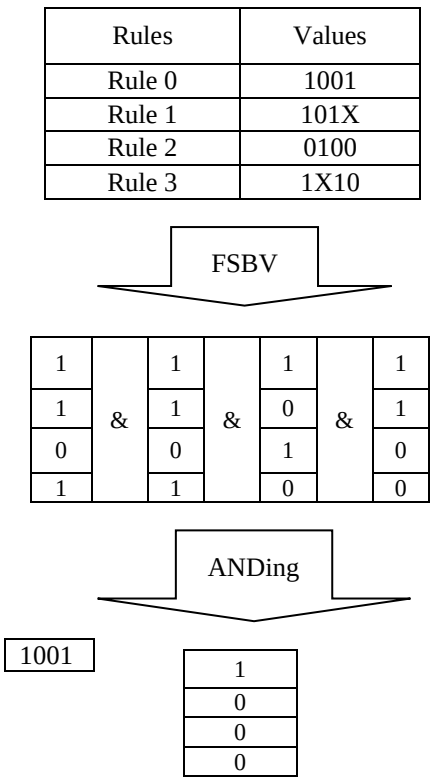

Figure 1. Field Split Bit vector Algorithm Match

The aim of an algorithm is to find a matching rule for the incoming packets, to make bit vector of the same size as that of rules, and then AND the results of all matches.

The algorithm output is the corresponding rule number. The need for a high-speed packet classification also increases as network speeds increase. In order to achieve wire speed treatment and avoid unauthorised attacks, constant time complexity is normally required. The packet classification means the reception by the network of a data, certain pre-defined fields, and the performance of a type of action defined by the classification declaration corresponding to the fields of the incoming packet. The core of the packet classification is the set of rules defining a certain classification. All fires are part of the common operation set for a firewall. The most frequent firewall rules are semantics. A firewall allows action means that the packet should be transferred to the network to its destination and denies that the packet should be dropped and the firewall not allowed. The order is normally dictated that the first rule is more prior to the second rule, etc. The packets are called packet classification in an internet router. For best efforts such as firewall and service quality, the classification of packets is necessary to ensure proper networking and avoid unauthorised access. Generally speaking, multi-field packet classification is a difficult problem [6]. The memory is decided on flow, rules are matched and action is taken according to the priorities of the incoming packet. Researchers have therefore declared a number of packet classification algorithms.

3. Previous Work

Innovative scalable architecture [5] and modular classification methods have been developed by Thilan Gara, Weirong and Viktor Prasanna. They proposed a new, bit-vector FPGA (FPGA) architecture using modular, field-programmable logic arrays (FPGA). Because we must attempt to avoid the use of range conversion in architecture, the search engine will only search for solutions which support all the various match types. The architecture can be scaled to extract the highest priority encoder from the hardware. StrideBV does a stand-it-alone rule-based approach as the solution depends on the application and the solution can be a variety of ways to implement,

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flexibility is not necessary. According to the architecture, the proposed Xilinx FPGA device supports up to 28K rules, but uses on-chip resources to deliver up to 100+gbps of output, while delivering parallel and serial outputs. Both a decomposition-based and survey-based analysis is proved to be desirable approaches for classifying the package. For several years, topic of research and development is Packet classification-based firewalls that have been under active attack; their efforts are being directed toward building multi-party firewalls and all types of intrusion detection systems. Those who specialise in package classification are best suited to introduce package classification software. One-dimensional packet classification is a must with Ternary Content Addressable Memory (TCAM) in use. The TCAM search engine works on all parameters at high speed and precision. They suggest a Binary Reflected Gray Code (BRGC) method for multi-dimensional packet classification by means of range. The BRGC encoding scheme is mentioned but can be used to identify both the source and target port as well. By using the BRGC, we gained the ability to have limited scalability and increased the blowout range.

To increase the speed of packet classification [6], decomposition optimization was proposed by Lu Sun and Viktor Pras. Decomposition involves two steps: first, we conduct independent searches on each packet, and then we aggregate the results from the first step. Decomposition algorithms are common in artificial intelligence, in which a complex problem is broken down into simple sub-problems to be solved or processed and are called iterative algorithms. It would yield a better result if the additional rules and optimizations for the second phase of the algorithm were incorporated into the overall design. Compared to other decomposition based algorithms, the design is better; it's more efficient, workable, and more pleasing to the eye. The proposed design was built on Xilinx Virtex-6 XC6.X-2 with the target application in Verilog running on the ISE 12.4 design tool.

FSB (Full-Parallel Spread Bit) architecture has been invented by Jiang Weirong and Prasanna Victor Snort utilises the current FPGA and RAMs ; the FPGA RAM design is well-suited to the FSB architecture. In addition, it handles multi-match packets well. This FSBV architecture provided a frequency of 167 MHz, using dual-port ram on a Xilinx 200 Virtex-6 XCVT device enabled it to process two packets per clock cycle. Dynastic rule architecture package management for the FPGA design package class has been proposed by Yun, Viktor, Prasanna S. and Zhou Z. The architecture in use is designed to be process able in your own way. Modular processing [7] refers to modules that have the ability to handle both the matching range and the matching of a range. Dabbles, instead of a single architecture with a limited number of rule modules, to handle a large number of rules using several DPLs (PEs). The architecture takes striding and clustering [8] into account the varying rules. The architecture can use striding and clustering rules to identify the s-bit subset of the input data. To make alterations to, insert, remove, and insert your own, you can use a set of algorithms. You can update the hardware rules without slowing down the pipeline. The large architecture is expandable.

4. Proposed Work

Both bit vector and split fieldwork techniques are applied to classifying packets with the XNOR gate are utilised in this research paper. They are part of a collection management group with strong authentication for private network security and help to avoid unauthorised access. For most complex procedures, the required memory will depend on the number and size of rules. We use the bit vector algorithm and field split field comparison algorithm to examine rules and packets. We use the four rules listed above, 'one-to-one' and 'zero-to-one' to represent four data points. To keep track of incoming traffic, action is taken according to the standard. Instead of comparing the total size, each time an inbound packet matches a rule, use the base x-nor rule to match all inbound packets to it, calculate a result for each match and apply it. The input packet status for each bit of the rule is also provides to each following bits in the

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rule set. A priority encoder is employed for identifying a high-priority rule. The highest priority rule in the rule set is selected by priority encoder.

20-bit incoming packets:-

Eg- 10011010100110011001

Rules- 0 1 0 0 0

Packet select= 1001 & select rule= 0

Eg- 01000100101001001010

Rules- 2 2 1 2 1

Packet select= 0100 & select rule=2

A search table with a height and width in each row is stored on a memory equal to number of rules (N). An N-bit vector from the appropriate memory location contains the corresponding outcome of rules with incoming packets. We performed packet classification with the basic x-nor gate in this paper. The advantages of the modern packages processing system are high speed and the capacities to cross multiple layers, which make it a known method for packet classification instead of demultiplex. Our proposed packet classification method is efficient for the same number of rules and requires less memory for the research table.

5. Design Methodology

Figure 2 shows the proposed work architecture for the 104-bit packet header. For incoming packets, use the header file. Incoming packets are used for the header files. There is a block number such as a rule set up lookout table, the separator block, XNORing (Exact), Comparator (Range), ANDing and the Bit-Vector generator block. All blocks indicate that the operation of the Bit-Vector Field Split depends on the rules of incoming packets. The same bits match here and different bits do not match as the XNORing operation performed. After XNORing, the ANDing operation is executed and the top rule sets are selected. Architecture shows a complete package classification top level system with XNOR gate and prefix or precise match and range match comparator.

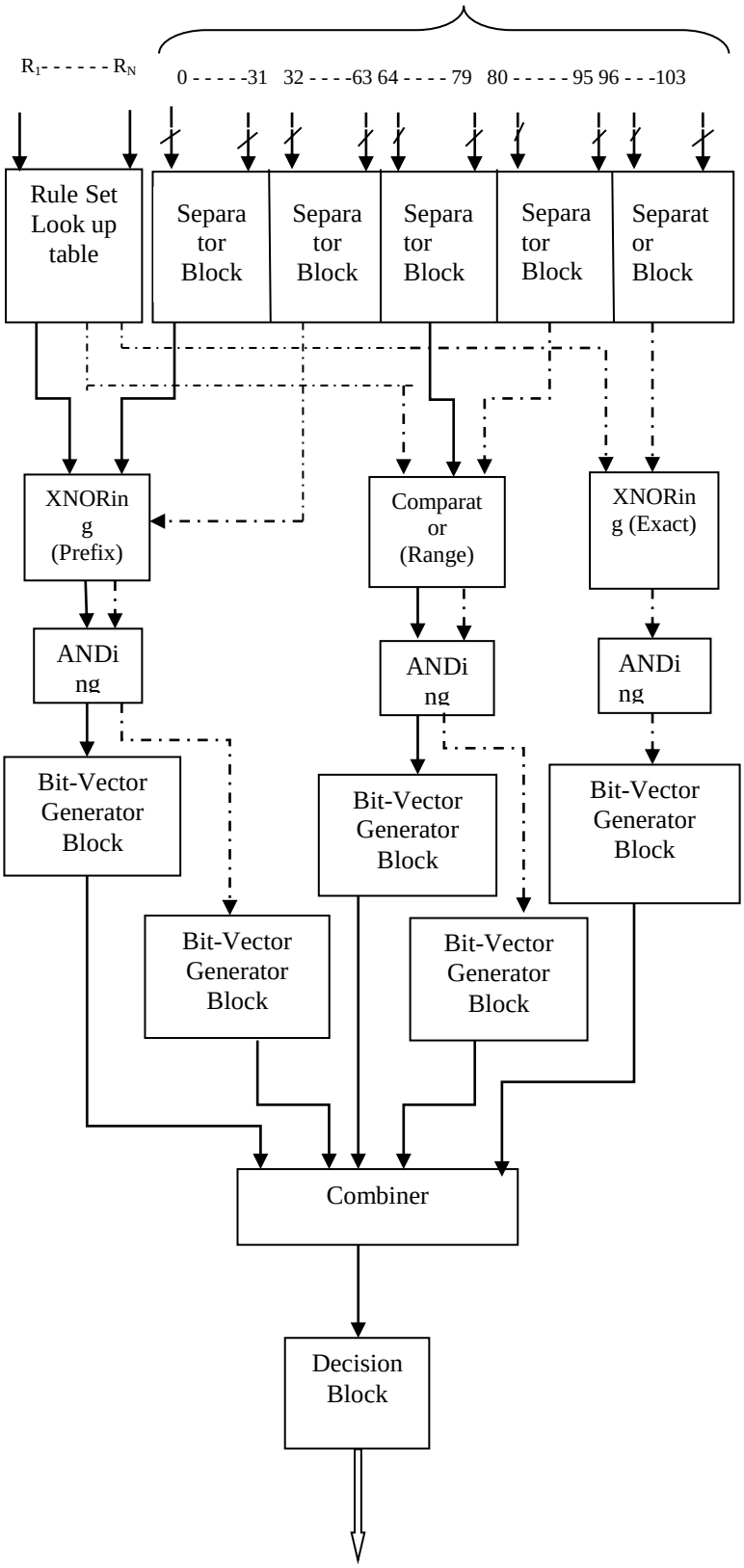

Figure 2. Proposed Architecture

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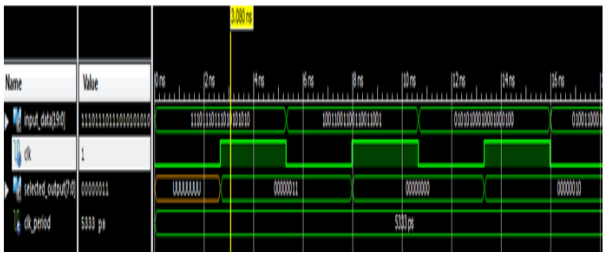

Figure 3. Stimulation result of 20 bit FSBV

6. Results and Discussion

Figure 1 shows the simulation outcome of FPBV. Packets and rules entered here are inputs that must be classified. Involving packets vector signal indicates a set of rules for status. Least Significant Bit (LSB) is the output of the result of the first FSB rule. The new method has been demonstrated. Stimulation result of proposed method is shown in Figure.2; input is field value and out status gives matching result of incoming packet. Most significant bit (MSB) of out status represents status of first rule of a rule set. In this paper, we use 20 bit and four rules, these rules are divided into five group, and matched incoming packet with rule is forwarded according to the highest priority match rule.

Table 1. Device Utilization Summary

Family :- Spartan6		
Target device :- 6slx4tqg144-3		
Rules-4, Packets-20 bit		
Memory-20 bit/rule		
Features	**FSBV**	**Proposed**
Latency	5.762 ns	3.597ns
Throughput	3.471Gb/s	5.560Gb/s
Memory	20 bits/rule	20 bits/rule

7. Conclusion

In the literature, there are different packet classification algorithms. The proposed approach is more optimized than existing approaches. It has higher throughput, is faster, and consumes less memory. It's first demonstrated in this study that the rules are all tested, and then the top rule is chosen. According to the work done in this paper, performance improvement in throughput is clearly observed. The rule length varies depending on the number of packets and the type of memory needed. The proposed algorithm has a latency of 3.597 n seconds.

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