DESIGN OF HIGH THROUGHPUT ADD COMPARE AND SELECT UNIT FOR LOW POWER VITERBI DECODER

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Abstract:

The main purpose of this paper is to focus on the design of Viterbi Decoder (VD) with low power, which is significant for receiver section of data communication applications such as Radar, Satellite, Telephone and Automatic speech recognition. The Viterbi decoder algorithm consists of three most important blocks – Branch Metric Unit (BMU), Add Compare and Select (ACS) Unit and Survivor Memory Unit (SMU). BMU computes the metrics between the input and output state transitions. ACS unit include the Path Metric Unit (PMU), which computes the metrics with the sequence to a next state of a path and selects the lower metric value as a survivor path. SMU stores the data bits which utilizes the trace back method to fetch the likelihood path from the current state to a previous state. An ACS unit is an essential block for VD. The basic recursive ACSU design consists of Ripple Carry Adder (RCA), Comparator and a Selector block, which consume more area, power and operates with high junction temperature. To overcome these drawbacks, a modified ACSU design is implemented with recursive cancellation technique. ACS unit is modified by including a trace back mechanism to obtain a low latency and high speed in VD. It is designed with low complexity multiplexers, adders, logical AND gate and comparator block. This breaking recursive ACSU design utilizes less power, high throughput, low latency and also operates at low temperature. This analysis and simulation process are accomplished using Vivado Design Suite.

Keywords:ACSU, Comparator, Convolution encoder, Recursive design, Viterbi Decoder

Introduction

Fast and reliable digital communication system has beenidentified and plays a vital role in today's life style.An error coding techniques has high demand, to access digital communication system of high bandwidth, which provides better performance. Data coding techniques plays an important role, to sustain high reliable data and to have abetter Bit Error Rate (BER) for digital communication systems[18].A convolution code is one of the Feedforward Error Correcting (FEC) codes, which frequently utilizes for encoding process of communication system[11].Binary convolution codes was first introduced in 1955 by Elias and further researches were done by many mathematicians. This encoder is a linear system, which depends on present and previous data input streams. For generating a convolution code, the data streamsare passed sequentially through a Linear Feedback Shift Register (LFSR). The encoder outputs are obtained based on generator polynomials via modulo-2-adder (XOR gate) with their respective register cells[7].Convolution codes can be systematic or nonsystematic, which usually consist of two parameters – code rate and constraint length. The ratio of the number of input symbols (k) to the output symbols (n) of the channel encoder is termed as code rate (r) and expressed as (r=k/n bits/symbols)[10]. The length of a convolution encoder is termed as constraint length (K).The encoder output is named as Encoder Output Sequence (EOS) which depicts the information of each shift register cell, where each register block was initialized with zeros at the first stage of an encoding process [3].This encoder block is placed in the transmitted section across the channel. The end of the channel may include a noisy sequence of bits with information, which is termed asan error. In order to decode that inaccurate information, a unique algorithm is developed by Andrew James Viterbi in 1967, which named as Viterbi algorithm. The Viterbi algorithm has an enormous demand to decode the convolution codes, even if the channel comprises a noisy signal as depicted in block diagram (see Figure. 1)

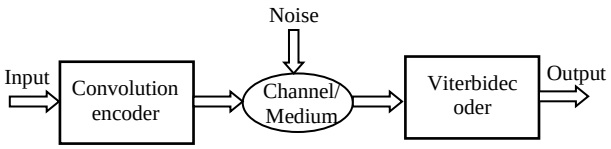

Figure 1. Block diagram of Convolution encoder and Viterbi decoder.

The viterbi decoder algorithm has a capability to operate with a high speed [19]. This algorithm computesa maximum likelihood sequence of state transitions, equivalent to a trellis encoding process by allowing the present transition metric to desirable state transitions.A

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transition metric is termed as branch metric, andthe path across each branch metric level is named as path metric. If the same state consist two or more path, then the smallest path metric is considered as the likely path. The survivor path is accomplished by the backtracing process which corresponds to the decoded output. However, this algorithm is logically complicate and consumes more power, but it is most relevant for decoding the convolution codes.The VLSI researchers were focused on power reduction of Viterbi decoder due to vast applications on communication process. A typical Viterbi decoder consists – Branch Metric Unit (BMU), Add Compare Select Unit (ACSU) and Survivor Memory Unit (SMU)[14].

ACS unit include Path Metric Unit (PMU), thus Viterbi decoder requires more power due to the ACS unit. Thus researchers were focused on designing low power and low complexity ACS unit using various methods such as T-algorithm, radix method with minimum stages, Hybrid Register Exchange Method (HREM), Exchangeless algorithms, Minimum transition algorithms, and by including Threshold gate unit[6][2][4].Hence this paper intentionis to design an ACS unit by including trace-back mechanismtobreak the recursionin a closed loop, which utilizes less powe high throughput, low latency, and better performancewithout disturbing the hardware complexity of Viterbi decoder.The proposedACS unit is significant forViterbi decoder, which is utilized in receiver section of communication system.

This paper is organized as follows. Section 2 describes the background of basic Viterbi Decoder (VD). Section 3 presents a brief explanation of non-recursive Viterbi Decoder (VD) and Section 4 discuss the simulation results. Section 5 concludes the paper.

Prior Work

In the present scenario, communication consists wide applications such as Data communication, Image processing, DSP and so on. As communication is a demandingprocess, encoding and decoding techniques play a crucial role for the transmitter and receiver section of a system.The operation of convolution encoder is a simple process which consistsof multiple shift register cells and modulo-2-adder(XOR gate). Fig.2 shows the functional diagram of Convolutional Encoder (CE) with ½ code rate[18].

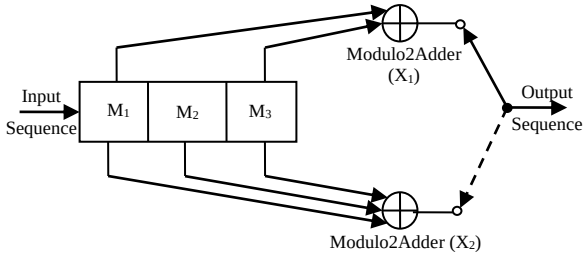

Figure 2. Functional block diagram of CE.

An input sequence is applied to the memory cells (M1, M2, M3) of 1-bit shift registers which are initialized with logic zeros[1][9]. The output of memory cells are assigned to modulo-2-adders (XOsR operation) based on generator polynomials, the desired outputs for CE with code rate ½ are X1 and X2 expressed as follows.

$$X_1 = M_1 \oplus M_3 \tag{1}$$

$$X_2 = M_1 \oplus M_2 \oplus M_3 \tag{2}$$

The generator polynomial sequences of the two adders are (Gi(1) and Gi(2), where i= 0,1,2,…..N). For example, message sequence (M) is (1101) and generator polynomials are (101 and 111) respectively, then the desired outputs.

$$x_i(1) = \sum_{i=0}^{N} g_i(1) * M = 1110 \tag{3}$$

$$x_i(2) = \sum_{i=0}^{N} g_i(2) * M = 1000 \tag{4}$$

By computing the equations (3) and (4), the final generated set of an encoded sequence is (11 10 10 00) for respective message bits [7]. To decode this expandable information bits, other error detection/correction technique is required at the destination point. The present trendy decoder is a Viterbi decoder algorithm, most sensitive to detect/correct the error [17].

Viterbi decoder

Viterbi decoder is a maximum likelihood decoding algorithm[1]. It is capable for reducing the Bit Error Rate (BER) to a great extent but flexible for only shortcodes[13].The basic block diagram of VD is shown in Fig. 3.

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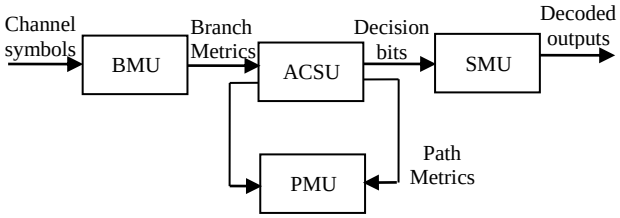

Figure 3. Top Module of Viterbi decoder.

The important block of Viterbi decoderare – Survivor Memory Unit (SMU), Add-Compare-Select Unit (ACSU) and Branch Metric Unit (BMU).The functional diagram of Viterbi decoder is shown in Figure 4.

Branch Metric Unit (BMU)

The first and smallest unit of VD is BMU, which utilizes the received codeword from an encoded channel [12]. It computes the Hamming distance or Euclidean distance for branch metrics of received bits and branch codeword [8]. The working of BMU is simply done with two logical exclusive-OR gates and 3-bit counter.

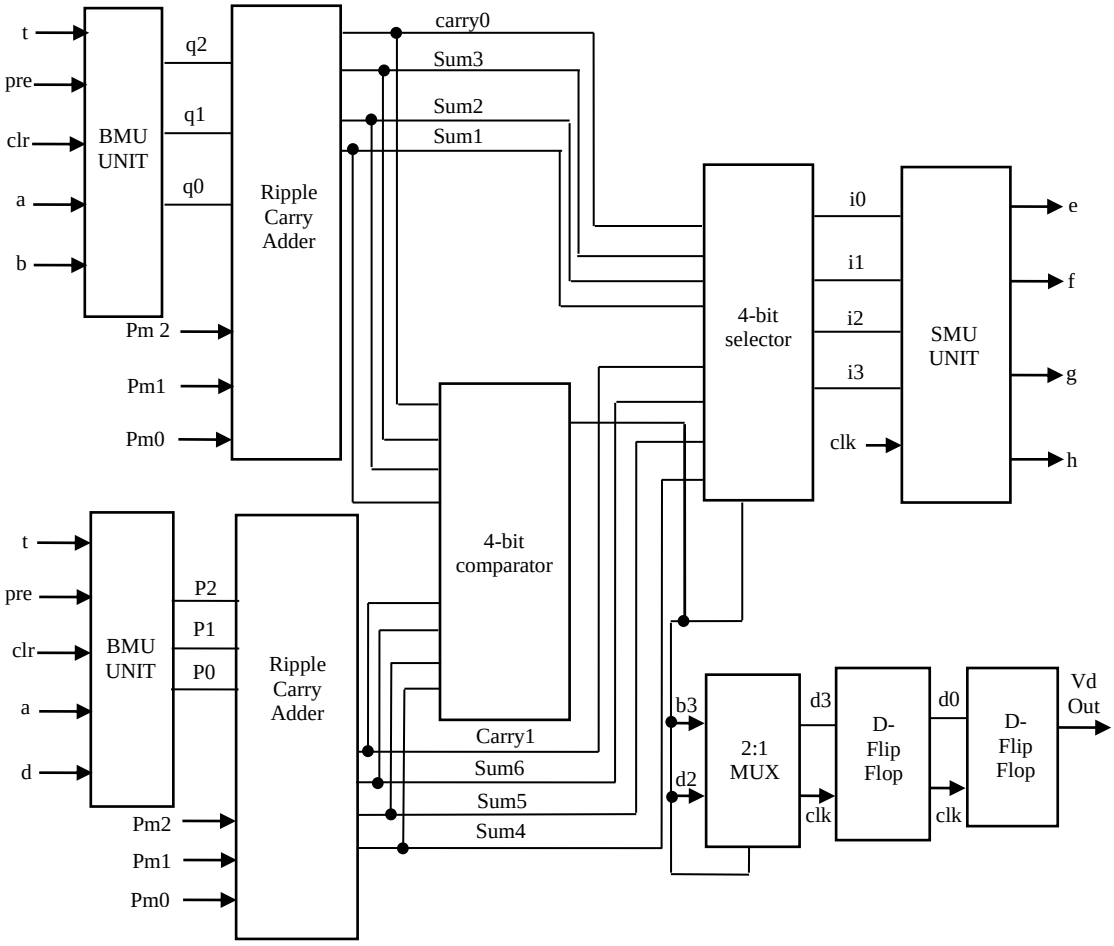

Figure 4. Internal architecture of Viterbi decoder.

Add-Compare-Select Unit (ACSU)

ACS unit is accommodated with Path Metric Unit (PMU), which computes a new Path Metric (PM) by adding branch metrics and encoded symbols from the previous stage of PMusing trellis method [5]. Now compares the new PM value of each sate and then stores the selected likelihood PM in the Path Metric Unit (PMU). The ACS unit allows the associated survivor path decisions and fetch the traceback pathby the Survivor Memory Unit (SMU). The PM of a survivor path of each state is evaluated and saved in PMU. To accomplish thebasic ACS unit, we require 3-bit Ripple Carry Adder (RCA), 4-bit comparator and 4-bit selector blocks as shown in Figure 4[16].

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Survivor Memory Unit (SMU)

SMU is a memory unit used to store the selected PM value from the previous states of ACS unit [20].There are two trendy methods toperform SMU unit – Trace Back (TB) andRegister Exchange (RE) method.RE method occupies more area compared to TB process, but requires less time to select the best survivor path, since it stores the PMs simultaneously. The drawback of RE process increases a routing cost with an increase in constraint length.Thus, mostly TB process is utilized to design viterbi decoders, which consume less area and low power[5]. There is no need of external resources even when constraint length increases, but the execution time is more to trace back the survivor path. The TB method is much ease and flexible for both soft and hard decision modes. Hence, the internal SMU unit is designed with 4 Serial-In Serial-Out (SISO) shift registers using D-flip flops.
The basic design flow forVD consists of three steps –

Proposed ACS Unit

Multiple arrays of ACS units are included in VD, which are interlinkedin a parallel form.Each ACS unit of an array operates in a serial mode with adder, comparator and selector blocks.Itis processed to implement an addition of BM values with PM metrics, next comparethe accumulated adder for each state and select the smallest PM value in a trellis state mechanism. These metric values are given to SMU unit, to store the history of shortest path metrics of each state and fetch the best trace back path. The basic ACS unit results in increasing the interconnections, utilize more power, more area, less speed. The existing ACS unit is a recursive (systematic) method, which repeats the process without consideringthenoise signal.

The breaking recursive (non-systematic) technique is an efficient method and has better noise immunity in processing multiple arrays of ACS units.Thus ACS unit is proposed with recursivecancellationtechnique, which has thekey challenge to attain low power consumption, high throughput, low latency and better noise immunity for VD. The modified ACS unit is comprisedof 2-bit Multiplexers, 2-input logical AND gates with single input negation, 2-bit adders and comparator.In this paper, three non-recursive ACS units in parallel modeare implemented but each unit access in serial . Figure 5 shows the 3 parallel modified ACS units (ACSU0, ACSU1 and ACSU2) of viterbi decoder[15].

Step 1. The initial stage, received bits from the transmitter source to BMU, which computes the Hamming distance for each state.
Step 2. When VD follows the trellis method, ACS unitutilizes the PMU block to compute the Path Metrics (PMs) frequently until the maximum likelihoodpath occurs.
Step 3. The final stage of the survivor path is to depict the decoded data, by traceback the shortest path metrics.
From the viterbi decoder, ACS unit is the main unit for computing/selecting the best PMsof each state, which improves the throughputand performance of VD. The existing recursiveACS unit is designed with normal RCA, comparator and selector, which consume more power and area complexity. It leads to the performance ofa Viterbi decoder. Thus, the following section is enhanced on breaking recursive ACS unit with low power, less area and high throughput.

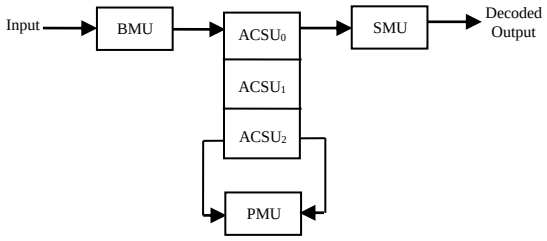

Figure 5. Block diagram of punctured Viterbi Decoder.

The modified technique is designed with constraint length (K)has multiple shift registers (M) in the trellis state mechanism of VD. Figure 6 shows the internal structure of singlestage non-recursive ACS unit. Where UP is termed as updated path, P is a path metric, BM is a branch metric.

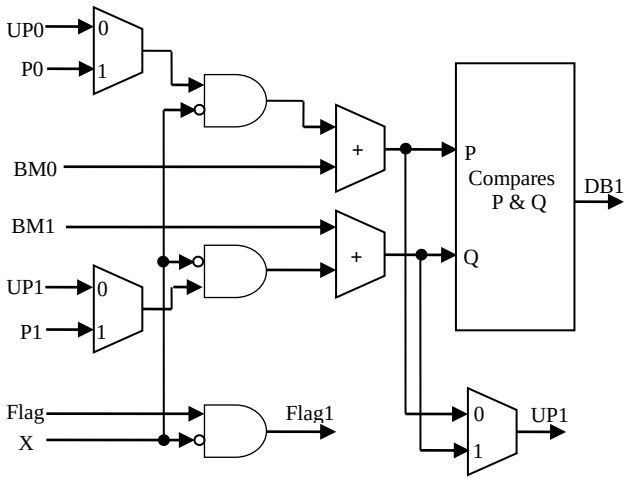

Figure 6. Architecture of ACS unit.

Thefunctioning of ACS unit is to add the BM valueswith the corresponding PM metric, next compare the updated

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PM values and then store the selected PM in the Path Metric Unit (PMU).The PM of the survivor path of each state will update and store in PMU. Simultaneously, ACS unit allows the survivor path decisions to Survivor Memory Unit (SMU) block. The same process is repeatedforthe modified ACS unitbut it is designed with 2:1 MUXs, AND gates, adders and comparator. The purpose of the MUXs is to select the path metrics, AND gate is to operate based on X signal. The 1-bit adder blocks are used to perform an addition operation of BM and selected PM value. A comparator block is used to compare the results of adder andstore the selected path metric in Survivor Memory Unit (SMU).

This modified breaking recursiveACS unit is ease to implement. Thus 3 ACS units are interconnected parallelly and implemented to verify the recursive cancellation technique.It consumes less power, high throughput, low latency and betterutilization compared to recursive ACS unit. Hence, this design is relevant for VD to have the advances of breaking recursive method.

Results & Discussions

The low power ViterbiDecoder is relevant for a receiver section of variousapplications such as Television, Cellular communication, Satellite communication, Radar and multimedia communication. Due to vast application for digital communication system, encoding and decoding techniques plays a crucial role for an error correcting/detecting the system. Convolution codes is a tremendous encoding technique which suitable for transmitter section.

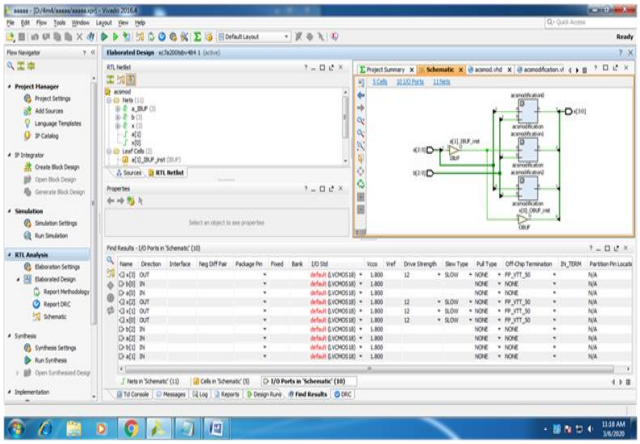

Figure 7.Schematic view of proposed ACS units

Similarly, Viterbi decoder algorithm is well suited for decoding the convolution codes, which is a maximum likelihood technique. The Add-Compare-Select Unit (ACSU) is a main block for decoding process. ACS unit consume more power compare to other blocks. Hence this paper focused on low power non-recursive ACS unit to reduce the logical complexity, power consumption and to improve the performance level. The existed ACS unit is designed with basic components of trellis state method. Figure 7 shows the RTL analysis and Fig. 8depicts the simulated results of proposed recursive breakingACS unit for the given inputs
A=010, B=010
Output X = 0101

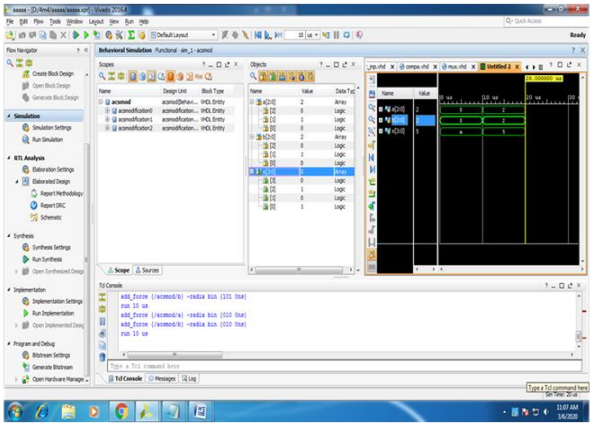

Figure 8.Functional response of modified ACS unit

The recursive cancellation ACS unit is designed with basic components like MUXs, single input negation of logical AND gates, adders, comparator provide less logical complexity compared to basic recursive ACS unit. Final report is listed below for the ACS block design of VD in Table 1.

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Table 1.Comparison table of ACS unit for VD.

	Basic ACS unit	Proposed ACS unit
Power consumption (w)	2.054	1.108
Junction temperature (°c)	30.3	27.9
I/O utilization (%)	4	2
LUT utilization (%)	1	0
Throughput rate	Low	High
Recursive cancellation	No	Yes

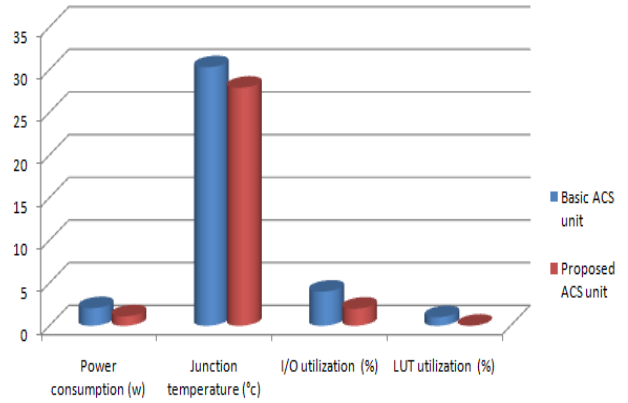

Figure 9. Comparison of basic and proposed ACS units

Conclusion and Future Scope

Viterbi Decoder (noise-free decoder) is highly essential for various applications such as Data communication, Image processing and Digital Signal Processing (DSP). In this paper, we have designed a modified approach for the ACS unit. The modified ACS unit has a capability of recursive cancellation technique in a closed loop, which consume less power, better noise immunity, low latency, less area utilization compared to existing recursive ACS unit. The 60% power and 50% area savings in proposed ACSU design is attained over recursive ACS unit.This low powerACS unit with recursive cancellation is utilized for large data processing applications. In order to minimize the power and increase the speed of viterbi decoder, various asynchronous delay insensitive methodologies may be adopted at ACS, BMU and SMU blocks. Delay Insensitive techniques minimizes the power by avoiding unwanted transitions.

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