The reduction of Crosstalk in VLSI due to parallel bus structure using Data Compression Bus Encoding technique implemented on Artix 7 FPGA Architecture

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***Abstract*— In this work, a bus encoding method is proposed that reduces the effect of crosstalk. The crosstalk usually occurs when the data is in parallel communicated. In planar structures, the crosstalk effect is large due to the usage of parallel communication and wide data patterns. In bus technique, the huge amount of wires is laid in equal over a significant time. One way to reduce crosstalk without changing the parallel communicating data lines is to reduce the wideband data patterns so as to reduce the power utilization. The proposed encoding method can minimize the crosstalk by reducing wide data patterns without degrading the performance. The architecture is implemented on Artix 7 FPGA at a 28nm technology node. The simulation is done using the HDL tool and the results are compared with the existing FPGA architecture. With the proposed method, the wire density and the power consumption are reduced by 57.4% and 50% respectively as compared with existing 45 nm technologies**.

Keywords — Data transmission, Crosstalk, bus encoding scheme, power consumption, VLSI, noise, propagation delay

I. INTRODUCTION

In telecommunication signals, crosstalk is an undesirable disturbance caused due to the electric or magnetic fields from the neighboring circuits which are known as electromagnetic interference (EMI). This problem also arises in microcircuits inside PCs and audio equipment in a network. The term is moreover applied to optical signals that interfere with each other [1]. Regarding electronics, the signal transmitted from one circuit is coupled with another circuit, which leads to undesirable effects named crosstalk. This is also the problem in speech

Signals leaking from other subscriber connections. If the signal propagation medium is analog the crosstalk effects are reduced by using twisted pair cable [2]. Another alternative is a signal conversion using ADC which is immune to crosstalk. In wireless communication, co-channel interference is the problem associated with crosstalk. During music recording process sound leakage from one instrument into a microphone placed before another instrument establishes the crosstalk. There are several sources to create crosstalk, one among them is due to capacitive coupling between the long length of transmission lines which results in unwanted voltage spikes in the neighboring buses. To minimize Crosstalk in fastest performance processor design using a bus encoding is given in [3]. A single wire has been associated with different types of capacitances where the capacitance 'C' is distributed between the wire and ground, and the other is the coupling capacitance C_c between the wire and its neighboring wires [4]. The C_c of each wire can be divided into C_1, C_2, C_3, and C_4(four types) according to the 'C' couple of two wires [5]. Forbidden Free Pattern is used to avoid the crosstalk given in [6]. The crosstalk-aware in-service optical path control system using single-mode multi-core fiber transport network introduced in [7]. The error controlling codes using 65nm CMOS technology and PTL with

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minimal performance parameters, codes based on novel pattern classifications are introduced in [8-9]. In worst-case, the crosstalk due to a large number of transitions in the group of lines is minimized using bus encoding scheme which reduce the redundancy and consumption of power [4]. Layout techniques are introduced to eliminate the problem of crosstalk competition presented in [10]. 14% of crosstalk is minimized using immune coding given in [11]. The V_{DD}, GND wires are added to a design layout between every signal wire proposed in [12]. Reducing the bus delay up to 75% by active shielding method which is a more forceful technique as compared to the passive shielding [13]. The optimal delay is achieved by inserting repeaters or buffers further which helps to minimize crosstalk introduced [14]. A physical design technique using statistical approaches requires accurate layout structure and repeater placement to reduce the average delay in circuit [15]. From literature, it was studied that all these techniques are needful for minimizing the average delay during data transmission using bus encoding method. In this work, a 28 nm technology generations of FPGA devices are used to reduce crosstalk in data transfer with less power consumption and with low delay. In this paper, an introduction to crosstalk and literature is discussed in Section I. The methodology of encoding and decoding are given in Section II. Section III deals with results and discussions and finally, conclusions are given in Section IV.

II. Methods of Bus Encoding and Decoding

II (a). Bus Encoding Methods

In Fig.1,the bus encoding blocks are given, which consists of the counter unit, controller, comparator, and three registers with the size of three bits. As shown in Fig.1, this structure accepts 7-bits input data and compresses them to 3-bit data as outputs in the following steps

- The coupling transitions among the 7- bit lines are identified by the number of zero's and one' s in controller and counter blocks.
- The output of the controller is high based on the maximum number of zero's or one's. The numbers of flips in the data lines are identified by comparing data lines of seven bits with the output line.
- Comparator output is set to high when the number of one's is less than the number of zero's and set to low vice-versa.

In general, the possible best cases are two, either all lines are in '0' or '1' state. The status of bit flip is stored in three-bit registers. So, the only maximum possible flips are three. If all the three register contents are zero, indicated that there are no bit flips leads to no crosstalk. The position of bit flips is shown in Table I.

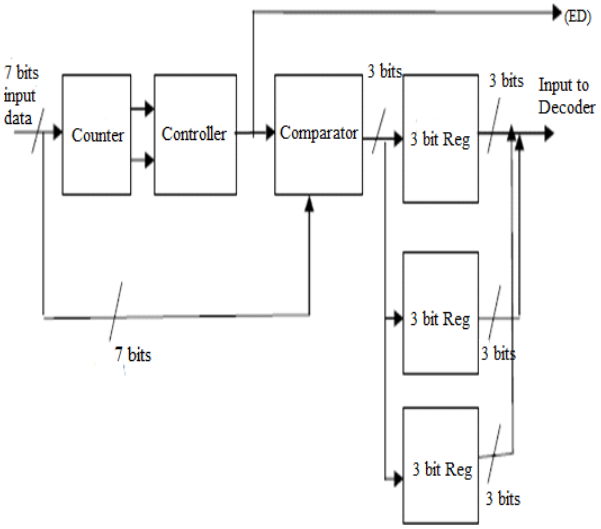

Fig. 1 Structure of encoding scheme

Table I. Flipped Line Positions with respect to Register Content

Content of register	Position of Flipped Line
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

The number of zero's and one's are identified by the counter unit in the input pattern by taking seven-bit input. Every input line is selected and compared with zero and one. The controller module is fed with two variables indicating for storing zero's and one' s in the input data. The comparator compares incoming data bit with the

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signal line and identifies the position of flipped bits and store the value in the three-bit register.

II (b). Bus Decoding Methods

The 3-bit output from the bus encoding logic is given to a 3-bit decoder with enable input as ED as shown in Fig. 2. The internal components of the decoder are three 3-bit registers, splitter, line-identifier, and an inversion module. For each clock cycle, new data is loaded with each of the registers and a three maximum clock cycles are needed for the decoding process. The function of the splitter is to map 1-bit input to 7-bits like de-multiplexer. The line to be flipped is identified by line identifier as it takes the data input from three registers. The final decoded output has 7-bits appear at the output after three clock cycles.

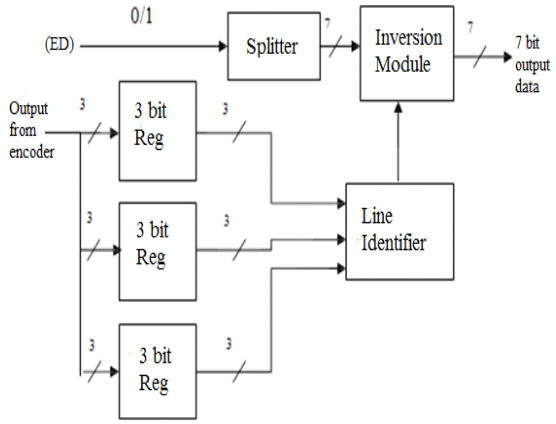

Fig. 2 Block diagram of decoder

III. Results And Discussions

The designed encoder and decoder modules are modeled using HDLs. The functional verification is carried out using Xilinx Vivado and implemented using Artix 7 FPGA at 28nm technology node. Xilinx XPOWER Analyzer is used to get the power consumption of the designed modules for various clock frequencies with different device families of FPGA. Fig. 3(a), shows the functionality of the encoder is depicted. The given input data to the encoder is "0101011" and output obtained as register contents as the state. Similarly, in Fig.3 (b) the functionality of the decoder is given in which the three-bit input "100" is decoded into 7-bit output as "0101011". The combined verification of encoder and decoder is presented in Fig. 4.

A. Simulation Results

Fig. 3(a) Simulation Wave form of Encoder (b) Simulation Waveform of Decoder

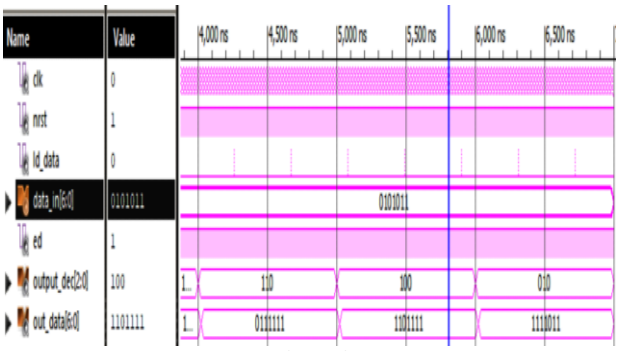

Fig. 5 Simulation Waveform of Encoder-Decoder

The area utilization in terms of the number of logic blocks, IO blocks, timing report of the designed encoder, decoder, and encoder-decoder modules are obtained from the synthesis report. The detailed synthesis reports of the encoder and decoder are given in Table II to Table IV.

B. Synthesis Results

Table II. Synthesis Report of Encoder

Device Utilization Summary of Encoder		
Devices selected :	7a100tcsg324-3	
Slice Logic Utilization		
Slice Registers:	30 utilized out of 126800	0%
Slice LUTs:	51 utilized out of 63400	0%
Number used as Logic:	51 utilized out of 63400	0%
Slice Logic Distribution		
LUT Flip Flop pairs used:	57	
unused Flip Flop:	27 utilized out of 57	47%
unused LUT:	6 utilized out of 57	10%
fully used LUT-FF pairs:	24 utilized out of 57	42%
unique control sets:	5	
IO Utilization		
IOs:	14	
bonded IOBs:	14 utilized out of 210	6%
Specific Feature Utilization:		
Number of	1 utilized out of 32	3%

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BUFG/BUFGCTRLs:	
TIMING REPORT	
Total	0.386ns (0.000ns logic, 0.386ns route) (0.0% logic, 100.0% route)

Table III. Synthesis Report of Decoder

Device Utilization Summary of Decoder	
Selected Device :	7a100tcsg324-3
Slice Logic Utilization:	
Number of Slice Registers:	31 utilized out of 126800 0%
Number of Slice LUTs:	26 utilized out of 63400 0%
Number used as Logic:	26 utilized out of 63400 0%
Slice Logic Distribution	
LUT Flip Flop pairs used:	42
unused Flip Flop:	11 utilized out of 42 26%
unused LUT:	16 utilized out of 42 38%
fully used LUT-FF pairs:	15 utilized out of 42 35%
unique control sets:	7
IO Utilization	
IOs:	13
bonded IOBs:	13 utilized out of 210 6%
Specific Feature Utilization:	
BUFG/BUFGCTRLs:	1 utilized out of 32 3%
Timing Report	
Total	0.640ns (0.361ns logic, 0.279ns route) (56.4% logic, 43.6% route)

Table IV. Synthesis Report of Encoder-Decoder

Device utilization summary of Encoder-Decoder	
Selected Device :	7a100tcsg324-3
Slice Logic Utilization	
Number of Slice Registers:	68 utilized out of 126800 0%
Number of Slice LUTs:	100 utilized out of 63400 0%
Number used as Logic:	100 utilized out of 63400 0%
Slice Logic Distribution	
Number of LUT Flip Flop pairs used:	130
Number with an unused Flip Flop:	62 utilized out of 130 47%
Number with an unused LUT:	30 utilized out of 130 23%
Number of fully used LUT-FF pairs:	38 utilized out of 130 29%
Number of unique control sets:	11
IO Utilization	
Number of IOs:	17
Number of bonded IOBs:	17 utilized out of 210 8%
Specific Feature Utilization:	
Number of	1 utilized out of 32 3%

BUFG/BUFGCTRLs:	
TIMING REPORT	
Total	0.645ns (0.361ns logic, 0.283ns route) (56.0% logic, 44.0% route)

The RTL schematic of the encoding and decoding bus is given in Fig. 6. Power analysis is carried out for the designed module at various clock frequencies and families of FPGAs using XPA. The timing path for bus encoding and decoding is obtained as 0.645ns targeted to Artix 7 FPGA and verified with different device families and the results are given in Table V

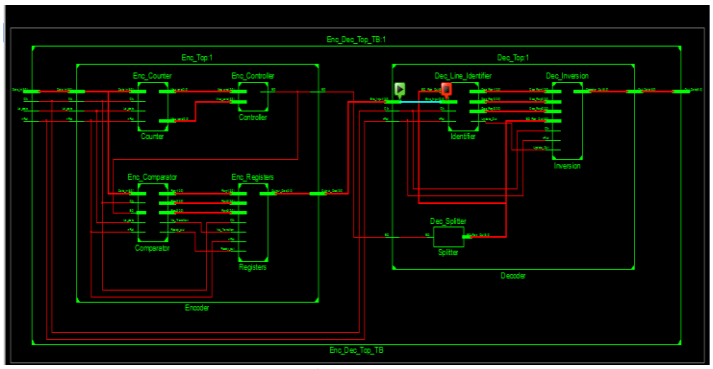

Fig. 6 RTL Schematic of Encoder-Decoder

Table V. Power Consumption, Delay Product and Power Delay Product for Different FPGAs at 500 MHz

FPGA device	**Power Consumption (µW)**	**Delay(nS)**	**Power-Delay product (f W-S)**
Spartan6	10660	5.05	53833
Spartan6 Low power	9230	5.05	46611.5
Virtex7	7780	0.511	3975.58
Virtex6 Low power	24240	0.68	16483.2
Artix7 (proposed)	**5350**	**0.64**	**3424**

From Table V, it was observed that Artix 7 consumes less power as compared with other FPGA device families. Note that other than Artix 7 is 45 nm technology. In high-performance processor applications, the Power Delay Product (PDP) is the most important design metric to indicate the performance of the design which is shown in the same Table V

The amount of consumed power of the proposed bus encoding is further compared with the existing works and is given in Table VI. Finally, it was observed that the encoding method at 28nm technology node the consumption of power is lowered as compared with existing works. The obtained results of 28nm technology

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bus encoding method have been compared with different techniques used for minimizing crosstalk.[16-19].

Table VI. Power Results of Bus Encoding Method are Compared With Existing Works

Technology	Method	Power(nW)
45nm	Existing- I [16]	43375.53
	Existing- II [17]	40214.31
	LUT-BED[18]	706397
	LUT-BED-CLA-[19]	26821
28nm	**Bus Encoding method**	**10000**

IV. CONCLUSION

In this work, the bus encoding method has implemented in HDL code.It has done to avoid the crosstalk noise(in decoder). The worst-case crosstalk is significantly eliminates or reduces by using this method. By reducing the number of lines from 7 bits to 3 bits for the output of the encoder crosstalk is minimized. Due to this, the crosstalk effectively minimizes on and average to 50%. In the end, the outputs of both encoding and decoding are the same without any noise. The signal transitions in wires indicate the functionality of the switching and coupling activities which helps to reduce the consumption of power and crosstalk. Finally, it was concluded that the power consumption of 57.4% is reduced as compared with other encoding methods. Further, this may also vary depending on the chosen style of FPGA.

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